An Improved Sigma-Delta Modulator for Digitizing Carrier Band Measurements

by

John Gerard Puskarich

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Author .....
Department of Electrical Engineering and Computer Science
May 19, 2005

Certified by .....
James K. Roberge
Professor of Electrical Engineering
Thesis Supervisor

Certified by .....
Eric M. Hildebrant
Principal Member Technical Staff, C.S. Draper Laboratory
Thesis Supervisor

Certified by .....
Shida I. Martinez
Senior Member Technical Staff, C.S. Draper Laboratory
Thesis Supervisor

Accepted by .....
Arthur C. Smith
Chairman, Department Committee on Graduate Students

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Abstract

Draper Laboratory currently employs a third-order Sigma-Delta modulator to digitize the outputs from microelectromechanical sensors at the intermediate frequency prior to demodulation inside a field programmable gate array. This modulator, which is built on a $.5\mu m$ CMOS process, is to be used as a standalone chip or as a core for use in larger microelectromechanical sensor integrated circuits. In this document, I submit the design of an improved Sigma-Delta modulator, which has a noise floor of $40\text{nV}/\sqrt{\text{Hz}}$ and a 5V_{pp} input range.

Thesis Supervisor: James K. Roberge
Title: Professor of Electrical Engineering

Thesis Supervisor: Eric M. Hildebrant
Title: Principal Member Technical Staff, C.S. Draper Laboratory

Thesis Supervisor: Shida I. Martinez
Title: Senior Member Technical Staff, C.S. Draper Laboratory

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John G. Puskarich

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Chapter 1

Introduction

1.1 Overview

Integrating the latest advances in electronics and mechanics, microelectromechanical systems (MEMS) technology allows for the realization of complete systems-on-a-chip. MEMS serve as an enabling technology for a vast array of applications from automotive airbag deployment to hazardous chemical detection. Taking advantage of these systems' ability to sense, control and actuate on the micro scale, the Microelectronics Group at Charles Stark Draper Laboratory constructs high performance instrumentation devices, specifically accelerometers and gyroscopes.

Our salient performance metric for these sensors is their resolution. Here we define resolution to be the minimum detectable change in acceleration or rotation that can be detected by the instrument. In recent instrument iterations, a portion of the signal processing that is responsible for sensor control and readout has been brought into the digital domain. This digital processing enhances sensor resolution by eliminating drift and noise due to the physical parameters of the electronics devices that we would be susceptible to in the analog domain. Additionally, such processing removes errors due to offset and signal degradation over various computation stages and across temperature.

1.2 Analog-to-Digital Conversion

In this environment where both analog and digital processing is being performed, there is a need to digitize an analog waveform. The accuracy (i.e. number of bits) with which we are able to quantize our signal governs the maximum precision of the output of the sensor's digital computation block. Figure 1-1 approximates the power spectrum of the analog input to be converted. In our application, the signal of interest is bandlimited to 200Hz about a carrier whose frequency is f_0, which is nominally 20kHz.

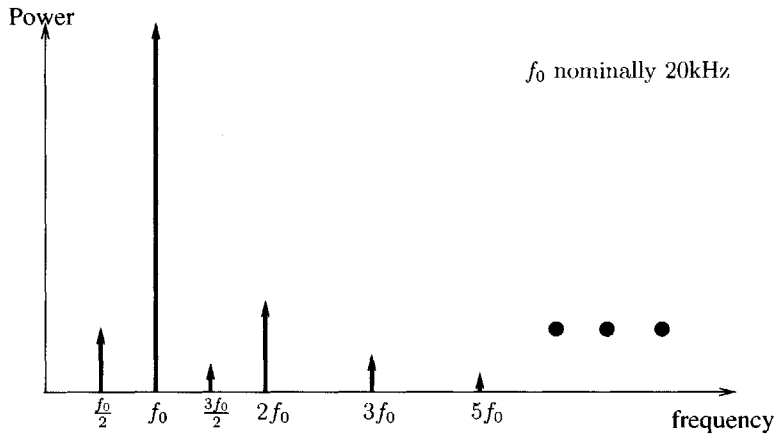

Figure 1-1: Power spectrum of input signal to be digitized

From the power spectrum of our input signal, we can extract two key specifications for the design of our analog-to-digital (A/D) converter. First, we desire the second harmonic distortion of the converter be very low to reduce distortion from $\frac{f_0}{2}$ on the amplitude of the carrier frequency . And secondly, we require that the noise of our converter be very low in the area of our signal of interest to keep conversion errors small.

To realize the digitizer, we choose to implement a Sigma-Delta ($\Sigma\Delta$) A/D converter. $\Sigma\Delta$ converters have become ubiquitous in modern VLSI technologies. These oversampled data converters have several advantages over conventional Nyquist rate converters, the most important of which is that they commonly employ a single-bit quantizer. This feature makes them inherently linear and very insensitive to compo-

nent mismatch, which has become a major design consideration with the scaling of today's technology.

In its mixed-signal instrumentation sensors, Draper Laboratory currently employs a third order discrete-time $\Sigma\Delta$ converter, which has an analog portion that has been designed and fabricated in a .5μm CMOS process. Table 1.1 summarizes the major specifications of the analog portion of this converter along with the measured results in the laboratory [3]. The device is powered by a single 5V supply (VDD) and the input signal is centered about a virtual ground of 2.5V (MID). The current converter meets the conservative specifications set forth; however, its signal-to-noise ratio (SNR) is problematic as it limits achieving higher resolution on next generation sensors.

Characteristic	**Target Specification**	**Measured Result**
Clock Frequency	$256 * f_0$	-
Input Range	$4V_{pp}$	$2.5V_{pp}$
Second Harmonic Distortion	< -80dBcFS	-82dBcFS
Inband Noise Density	$80\text{nV}/\sqrt{\text{Hz}}$	$140\text{nV}/\sqrt{\text{Hz}}$
Full Scale SNR within 20kHz$\pm$100Hz	124dB	111dB
AC Gain Stability at 20kHz	1% over temperature	0.4% over temperature
Spurious Tones	< -80dBcFS	No tones in output spectrum
Power Consumption	-	40mW

Table 1.1: Specifications for $\Sigma\Delta$ Modulator and Measured Results from Laboratory Tests of the Previous Third Order Modulator

1.3 Research Objective

The objective of this thesis is to investigate the design of a $\Sigma\Delta$ converter with lower noise than the current 3^{rd}-order implementation. This will be achieved by optimizing the performance of the analog electronics contained within the converter. In this document, as in the literature, we will refer to the analog block as the $\Sigma\Delta$-*modulator*. A block diagram of the entire converter is shown in Figure 1-2. The $\Sigma\Delta$ modulator is fabricated on a different integrated circuit than the digital electronics. We choose to restrict ourselves to using the currently in place decimator to narrow the scope of this thesis. The implications of this decision will be discussed later.

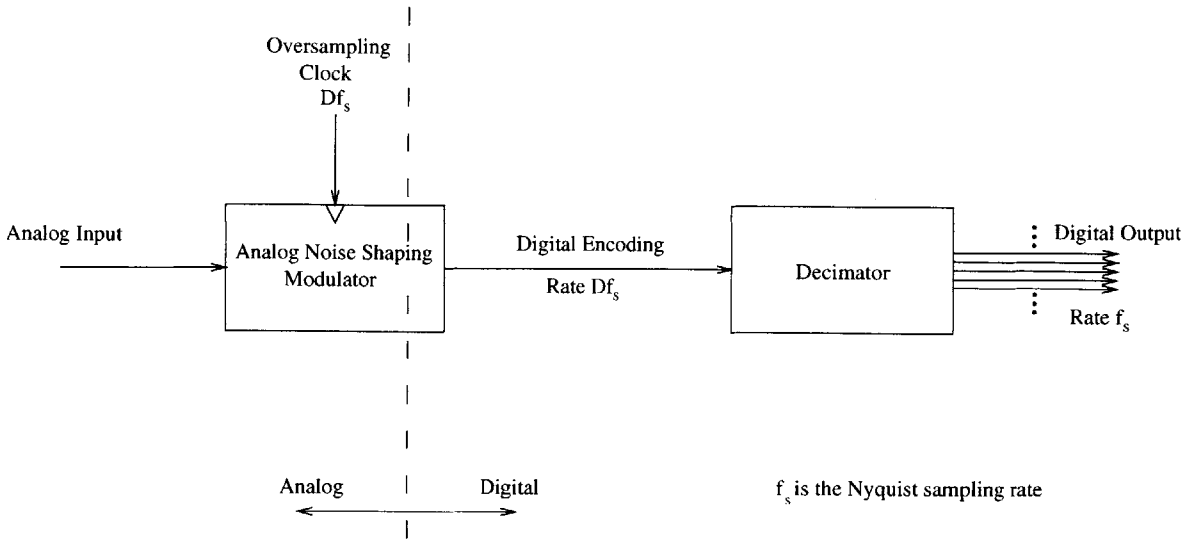

Figure 1-2: Block Diagram of a Sigma-Delta A/D Converter

1.4 Thesis Outline

The remainder of this thesis is organized as follows. Chapter 2 contains a detailed introduction to $\Sigma\Delta$ converters. This discussion will illustrate the numerous degrees of freedom that are available to the designer of such a converter. Chapter 3 presents the design methodology behind the previous third-order modulator, while pointing to areas where the architecture could be improved to obtain better performance. We begin to expound upon these areas in Chapter 4 where we construct a new loop filter for our modulator that more effectively shapes the quantization noise. Then in Chapter 5, we propose a new integrator structure that reduces the impact of the opamp's flicker noise and mismatch on the inband noise level. Finally, Chapter 6 details our results and makes suggestions for future work.

Chapter 2

An Introduction to $\Sigma\Delta$ A/D Conversion

In this chapter, we explore the features, operation and variants of $\Sigma\Delta$ converters. We do this by first discussing converter terminology and performance metrics within the context of an ideal A/D converter. Then, we explain why one would choose to implement a $\Sigma\Delta$ converter to achieve the A/D for our specific application over the numerous other architectures that have been developed. Continuing, we detail the main principals behind $\Sigma\Delta$ conversion to develop an intuitive understanding of such a converter's operation. Finally, we present $\Sigma\Delta$ architectures that are capable of achieving the level of performance demanded by our application at Draper Laboratory.

2.1 The Ideal A/D Converter

The purpose of an A/D converter is to transform any continuous-time analog quantity such as a voltage or current into a discrete-time series of N-bit digital words [7]. Figure 2-1 depicts a very basic block diagram of an A/D converter. Here, the analog input voltage, V_{IN} is converted into N-bit words by the relation:

$$D = \frac{V_{IN}}{V_{FS}} = \frac{b_1}{2^1} + \frac{b_2}{2^2} + ... + \frac{b_N}{2^N} + \epsilon \tag{2.1}$$

where b_1, b_2 and b_N are bits that take on value 0 or 1 and ϵ is the quantization error.

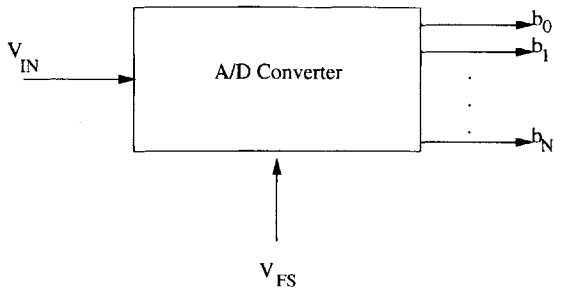

Figure 2-1: Simple Ideal A/D Converter Block Diagram

The transfer characteristics of an ideal 2-bit converter are shown in Figure 2-2. As we can readily see, the transfer function is discontinuous and does not exhibit a one-to-one relation between the analog input voltage and the digital output word. Rather, the output is a *quantized* version of our analog input voltage. The result of this attribute is that each output word corresponds to a small range ΔV $(= \frac{V_{FS}}{2^N})$ of input voltages. Hence, any A/D converter has an irreducible error associated with the conversion process. We refer to this effect as quantization noise, and it accounts for the fact that the analog input and output can be in error by as much as ΔV at any point (Note: In this document, we use the terms *quantization error* and *quantization noise* interchangeably) [9].

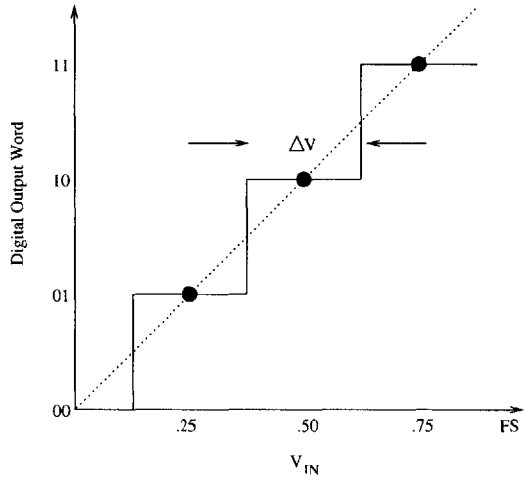

Figure 2-2: Ideal 2-bit A/D Converter Transfer Function

Let us now look at the error inherent in the A/D conversion process. The analog input to our 2-bit ideal A/D converter is a voltage ramp with slope equal to one. In Figure 2-3, we graph the error voltage (input voltage minus output voltage) and see that this varies between $\frac{\pm\Delta V}{2}$. The average value of this noise source is zero and its RMS value is given by the relation

$$V_{q,rms} = \frac{\Delta V}{\sqrt{12}} = \frac{V_{FS}}{2^N(\sqrt{12})} \tag{2.2}$$

Thus, we see that the amount of quantization noise present is proportional to the number of bits and some reference voltage V_{FS}. The figure of merit for our application is the converter's SNR. With this consideration in mind, we determine the SNR of an ideal 20-bit A/D converter with a broadband, sinusoidal input. At maximum, the input wave scales from 0 to V_{FS} with RMS value $\frac{\sqrt{2}}{2}V_{FS}$. This input yields the maximum SNR achievable by our converter:

$$SNR = 20\log\frac{V_{s,rms}}{V_{q,rms}} = 20\log\frac{\frac{\sqrt{2}}{2}V_{FS}}{\frac{V_{FS}}{2^N\sqrt{12}}} = 20\log 2^{20}\sqrt{1.5} = 122.2dB \tag{2.3}$$

Notice that this maximum SNR will increase by 6dB for each additional bit that we add to our converter. More importantly, note that this SNR calculation is only for the case when the converter's noise is solely due to quantization, which is the situation in an ideal converter.

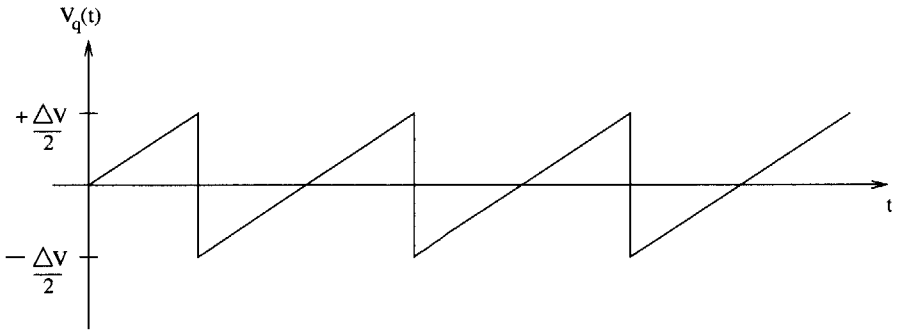

Figure 2-3: Ideal 2-bit A/D Quantization Error to Unit Ramp

2.2 Methods of A/D Conversion

A vast array of A/D conversion techniques have been developed. The selection of a particular conversion technique largely depends on the intended application. In certain instances, the governing parameter is accuracy, while in others speed of conversion takes precedence. These often conflicting requirements ultimately determine the choice of A/D conversion architecture that is utilized. Generally speaking, one can say that precision is obtained at the expense of conversion time [7]. Table 2.1 shows a number of different A/D architectures categorized by precision and speed [5].

Low-to-Medium Speed High Accuracy	Medium Speed Medium Accuracy	High Speed Low-to-Medium Accuracy
Integrating Sigma-Delta	Successive Approximation Algorithmic	Flash Folding Pipelined

Table 2.1: A/D Conversion Techniques

As discussed in Chapter 1, our application at Draper Laboratory demands a system that achieves a high level of precision in converting audio band signals. This shifts our attention to the converter architectures on the left side of Table 2.1– Integrating and Sigma-Delta. Inherent to integrating converters is the fact that they require a large amount of time to obtain high resolution. For example, employing this type of converter with a clock frequency on the order of a few megahertz to achieve 14-bit precision restricts us to handling inputs on the order of a few hertz. In contrast, $\Sigma\Delta$ converters with a clock frequency of a few megahertz are capable of operating on signals in the kilohertz range with greater than 20-bit precision.

As a starting point for our examination of $\Sigma\Delta$ operation and what differentiates this type of converter from others, let us look at the core functions of any of the architectures listed in Table 2.1- anti-aliasing, sampling and quantization. These blocks are shown in Figure 2-4.

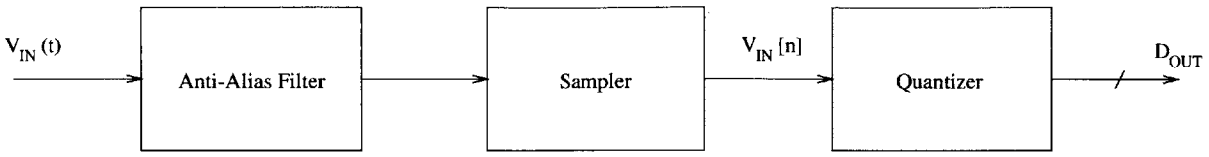

Figure 2-4: Block Diagram of A/D Core Functions

2.2.1 Anti-Aliasing and Sampling

The Sampling Theorem states that as long as we sample a signal (Bandwidth, f_B) at a frequency (F_S) greater than $2f_B$, the Nyquist rate, the original analog signal may be reconstructed exactly from its samples [4]. Thus, there is a need to band-limit a signal prior to sampling. Employing an anti-alias filter to band-limit our signal ensures that unwanted components such as noise and out-of-band interference do not fold into the $\frac{F_S}{2}$ baseband [1].

What are the requirements of an analog anti-alias filter for an A/D converter? Referring back to Table 2.1, we can classify a large number of these architectures as *Nyquist rate* converters. Nyquist rate converters generate a series of output values in which each value has a direct correspondence with a single input value. This class of converters operates at 1.5 to 10 times the Nyquist rate (i.e. F_S is 3 to 20 times f_B) [5]. Thus, this category of converters requires that the anti-alias filter exhibit constant gain over some passband (DC to f_B), rolloff sharply over a transition band (f_B to $\frac{F_S}{2}$) and then highly attenuate frequencies in a stop band (above $\frac{F_S}{2}$) as shown in Figure 2-5. The passband gain must be constant to the overall converters accuracy. And the attenuation of frequencies above $\frac{F_S}{2}$ must be such that the aliasing of such components into the signal band of interest does not affect the converter's accuracy.

Constructing these high-order analog filters is costly from a number of standpoints. First, their design is non-trivial as one must choose how well to approximate the desired filter response by choosing the number of poles and zeros that they will employ. This creates a tradeoff between the desired filter response and other key system specifications such as cost, power and size. Additionally, the performance of high order analog filters across temperature and process variation varies greatly due to the

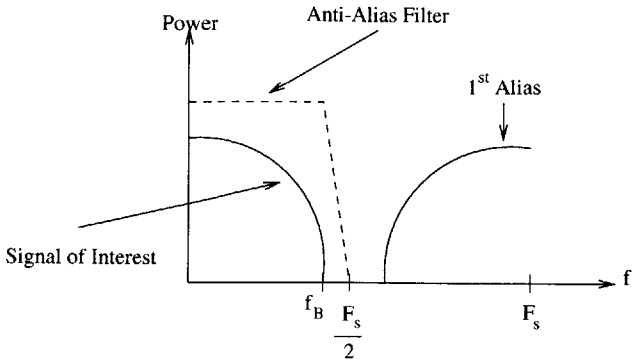

Figure 2-5: Spectrum of Input Signal after Anti-Aliasing and Sampling

physical characteristics of the IC fabrication process [1]. As we will soon see, we can relax all of these requirements by sampling at rate much higher than the Nyquist rate (i.e. $F_S >> 2f_B$).

2.2.2 Quantization

At the beginning of this chapter, we introduced the inherent quantization error in an ideal A/D converter from a time-domain point of view. To see how this error affects the spectrum seen in Figure 2-5 after it has gone through the quantizer block, we now look at the error from the frequency-domain standpoint.

In the presence of a continuously varying analog input voltage, it has been shown that the power of the quantization error can be approximated as a random voltage, uniformly distributed between $\frac{\pm\Delta V}{2}$ [9]. Standard $\Sigma\Delta$ analysis assumes that all of this quantization noise power, which is given by taking the square of Equation 2.2, will be spread over the range $[-\frac{F_S}{2}, +\frac{F_S}{2}]$ [5]. We show this quantization noise spectrum in Figure 2-6. This approximation for the spectrum of the quantization noise is commonly called the Additive Independent White Noise (AIWN) approximation. And it allows us the ability to model the quantizer's function as a linear element that simply adds in some quantization error $e[n]$ as shown in Figure 2-7. Note we are assuming that the quantization noise $e[n]$ is uncorrelated with the input signal $x[n]$. In actuality, these two signals have some correlation; however, for hand calculations this can be ignored and we can assume that $e[n]$ is broadband [5]. We can now take

the signal spectrum shown in Figure 2-5 as the input $x[n]$ to the quantizer and easily determine the spectrum of the output $y[n]$, which is shown in Figure 2-8.

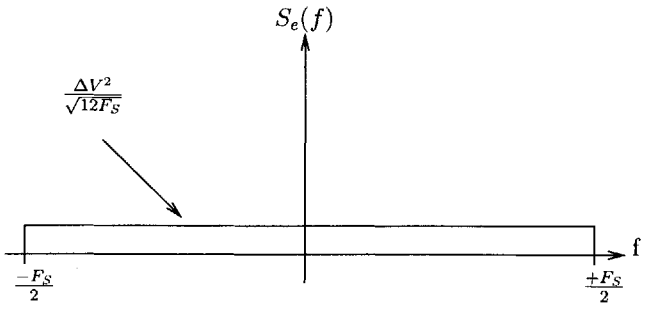

Figure 2-6: Quantization Noise Frequency Spectrum

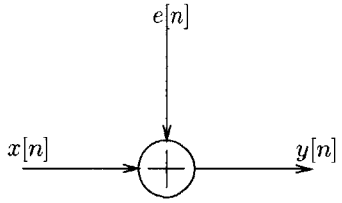

Figure 2-7: Linearized Quantizer Model

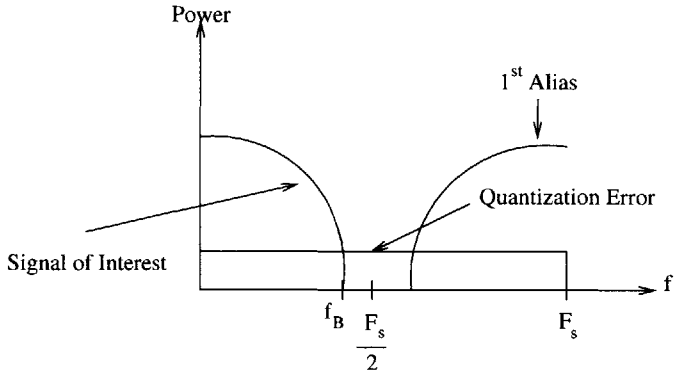

Figure 2-8: Spectrum of Output Signal after Anti-Aliasing, Sampling and Quantization

Now in calculating the converter's SNR, we only need to consider the quantization noise power (P_q) contained below f_B, since this is the band of our signal of interest. Because our input signal is sampled at about the Nyquist rate, P_q will not be dependent on the sampling frequency and Equation 2.4 yields a quantization power equal to that found in the beginning of this chapter.

$$P_q = \int_{-f_B}^{+f_B} \frac{\Delta V^2}{12F_s} df = \frac{\Delta V^2}{12} \tag{2.4}$$

Obviously the input signal power is concentrated below f_B, so if we assume this input to be sinusoidal, its RMS value is the same as before with power $P_s = V_{s,rms}^2 = \frac{V_{FS}^2}{2}$. This analysis yields an SNR:

$$SNR = 10 \log \frac{P_s}{P_q} = 6.02N + 3.01 \tag{2.5}$$

This is exactly the same SNR as we saw in the case of the ideal A/D converter with a unit ramp input voltage. We know this outcome should occur because the signal and quantization noise power fall within the same band [$-f_B$,$+f_B$]. Performing the analysis above allows us to look at a converter's SNR while considering finite signal bandwidth and a given sampling frequency in addition to the quantizer's resolution.

2.3 Oversampling A/D Conversion

To relax the requirements on our analog anti-alias filter and to reduce quantization noise in the band of our signal of interest, we now shift our attention to a class of converters that feature *oversampling*. Oversampling A/D converters operate at a speed much higher than the analog input signal's Nyquist-Rate. This increased rate is usually on the order of 10^1 to 10^3 times faster than required; however, these high oversampling rates restrict our converter to operating on low frequency signals. A generalized oversampling A/D converter block diagram is shown in Figure 2-9

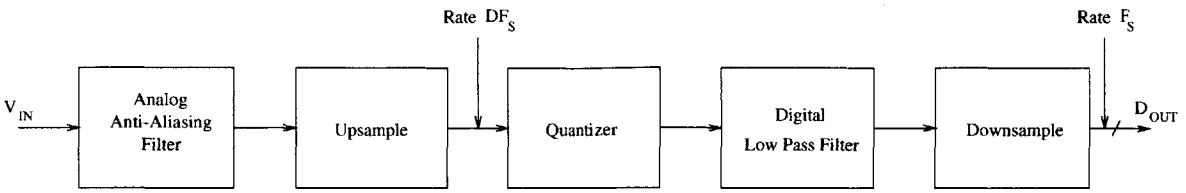

Figure 2-9: Generalized Block Diagram of Oversampling A/D Converter

2.3.1 Oversampling and Anti-Alias Filtering

Oversampling avoids the need for a steep-rolloff analog anti-alias filter as the first aliased signal is pushed up to around DF_S. We define D, the oversampling ratio as

$$D = \frac{F_S}{2f_B} \tag{2.6}$$

Figure 2-10 shows the frequency spectrum of our analog input signal that is now represented at a frequency far above the Nyquist Rate.

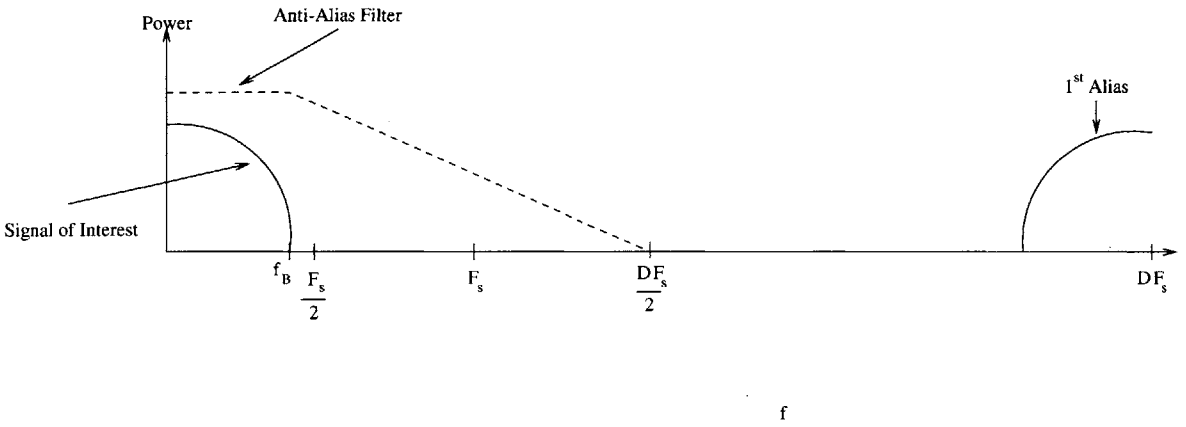

Figure 2-10: Spectrum of Input Signal after Anti-Aliasing and Oversampling

Noticeably evident from this figure is that the precision filtering requirements on our analog anti-aliasing filter have been greatly reduced. By reduced, we mean that we can now use an anti-alias filter with a much gentler rolloff. This is because our transition band has been expanded from $[f_B, \frac{F_S}{2}]$ to $[f_B, \frac{DF_S}{2}]$. However to accomodate the same final sampling rate, F_S, the oversampled signal must be further filtered to suppress frequencies above $\frac{F_S}{2}$ $(= f_B)$. The nicety we are afforded now is that this

requirement can be satisfied in the digital domain after the signal has gone through the quantizer. This enables much greater performance as high order filters are readily achieved in the digital domain.

2.3.2 Oversampling and Quantization Noise

As mentioned before, oversampling also serves to reduce the power of our quantization noise in the bandwidth of our input signal. In our discussion of the frequency spectrum of quantization noise, we saw that the power of this noise source is spread over the range $[-\frac{F_S}{2}, +\frac{F_S}{2}]$. When employing oversampling, we simply spread this power over a wider range of frequencies $[-\frac{DF_S}{2}, +\frac{DF_S}{2}]$. This change is shown in Figure 2-11.

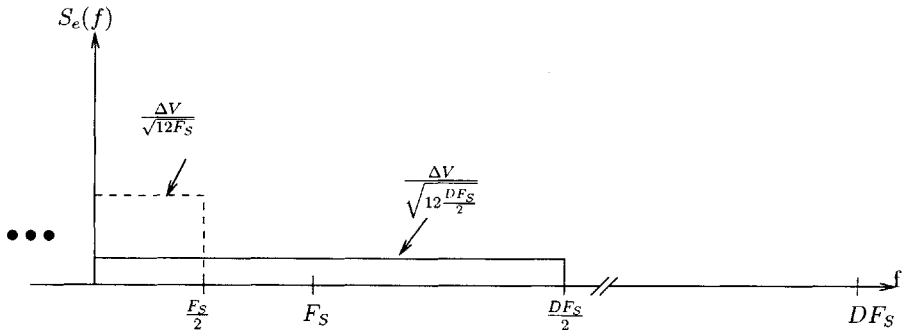

Figure 2-11: Spectrum of Quantization Noise after Oversampling - Negative Half of Spectrum Not Shown

Let us look at how oversampling affects our figure of merit, SNR. In the SNR calculation that we performed at the beginning of this chapter, we considered any sinusoidal input to our converter. However, in this instance, we choose to bandlimit our input signal to $[0, f_B]$. From before, the signal at the output of an N-bit quantizer with a sinusoidal input has RMS value $V_{s,rms} = \frac{\Delta V(2^N)}{2\sqrt{2}}$. So for a 1-bit quantizer, the output signal has RMS value $\frac{2\Delta V}{2\sqrt{2}}$. This value remains the same, as we assume the signal's frequency content is below f_B. However, the quantization noise power has been reduced:

$$P_q = \int_{-f_B}^{f_B} \frac{\Delta V^2}{12\frac{DF_s}{2}} df = \frac{\Delta V^2}{12D} \tag{2.7}$$

And we can see the resulting increase in SNR:

$$SNR = 10\log\frac{V_{s,rms}^2}{P_q} = 6.02N + 1.76 + 10\log D \tag{2.8}$$

Therefore, if our input signal is bandlimited to 20kHz and we require an output resolution of 20-bits, then according to Equation 2.8 we need to oversample to such an extent that our output SNR is 122.2dB. If we look to the case where we employ a 1-bit quantizer, we find that we must oversample at a rate of 8.6GHz to achieve our desired SNR. In the .5μm CMOS process that will be used to fabricate our converter, sampling at such a high frequency is not realistic.

A solution to the above problem is to use a quantizer with resolution greater than 1-bit. However, if we employ a multibit quantizer, then we introduce a high degree of nonlinearity. The reason for this is that oversampling does not improve the linearity of the quantizer. For example, if we had chosen to use an 8-bit quantizer in the example above, we would require that it possess an integral nonlinearity of less than $\frac{1}{2^{12}}$LSB. That is, the component accuracy would have to match to 20-bit accuracy. The major benefit of a 1-bit quantizer is that it can be highly linear as it only contains two output values [5]. This 1-bit quantizer is linear to the extent that the two output values are equal which means we must account for offset and gain error [11].

2.4 Noise Shaping

As an alternative approach to employing a multibit quantizer to realize a high SNR, we decide to shape the quantization noise through the use of negative feedback. In the literature, an oversampling converter that employs noise shaping and a 1-bit quantizer is termed a $\Sigma\Delta$ A/D converter. A general noise shaped $\Sigma\Delta$ converter and its linear model are shown in Figures 2-12 and 2-13. From an intuitive point of view, these systems are analogous to an operational amplifier utilizing negative feedback. If the op-amp has high gain in the band of interest, then the feedback reduces the effect of inband noise of the op-amp's output stage. Note that we have introduced a 1-bit

D/A converter in the feedback path in the block diagram seen in Figure 2-12. This component can be transformed into a unity gain block in the linearized model as it serves mainly to buffer the feedback signal to avoid loading the quantizer output.

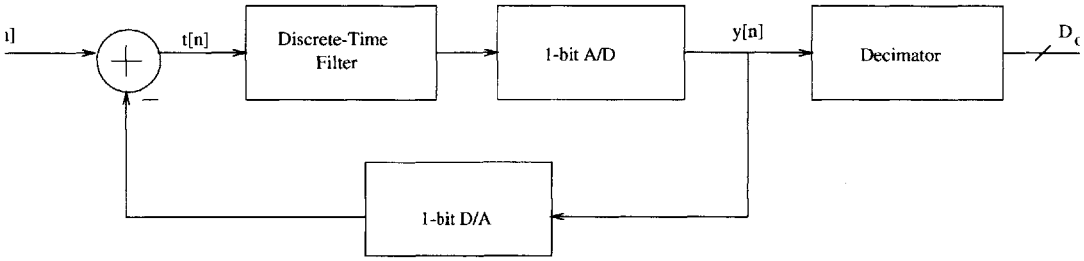

Figure 2-12: $\Sigma\Delta$ A/D Converter Block Diagram

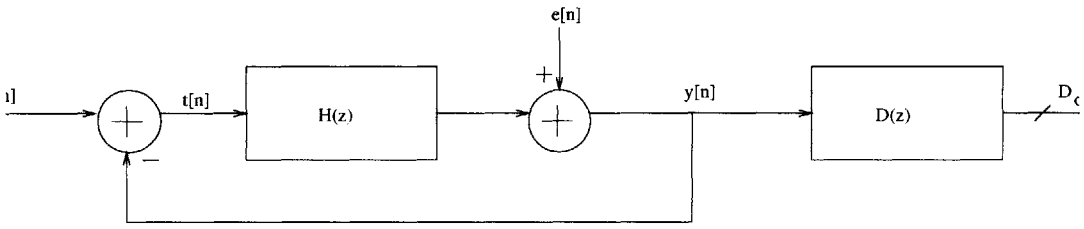

Figure 2-13: Linearized Model of $\Sigma\Delta$ A/D Converter

In Figure 2-13, $H(z)$ denotes the transfer function of a discrete-time analog filter. Treating the linear model shown as having two independent inputs (a result of our additive independent white noise approximation), then we can derive a signal transfer function, $S(z)$, and a noise transfer function, $N(z)$:

$$S(z) = \frac{H(z)}{1+H(z)} \approx 1 \text{ for } |H(z)| >> 1 \tag{2.9}$$

$$N(z) = \frac{1}{1+H(z)} \approx 0 \text{ for } |H(z)| >> 1 \tag{2.10}$$

To effectively shape the quantization noise, it is critical that the magnitude of $H(z)$ be large in the band of our signal of interest. This yields an $S(z)$ that is approximately unity over this band. Correspondingly this yields an $N(z)$ that will be roughly zero over this same band. Hence, the inband quantization noise power is

greatly attenuated. After digital filtering to eliminate out-of-band quantization noise, the frequency spectrum of our output signal will be approximately equal to that of our input signal.

Illustrating this technique, we plot the magnitude responses of $S(z)$ and $N(z)$ in Figures 2-14 and 2-15. If we know that the converter input will be low frequency ($D >> 1$), then we choose $H(z)$ to be an integrator. This will give us the desired effect that we just discussed– $H(z)$ has large gain for low frequencies and small gain for high frequencies. If we make $H(z)$ an integrator ($H(z) = \frac{z^{-1}}{1-z^{-1}}$), $S(z)$ is a pure delay with unity magnitude while $N(z)$ has a first-order high-pass response.

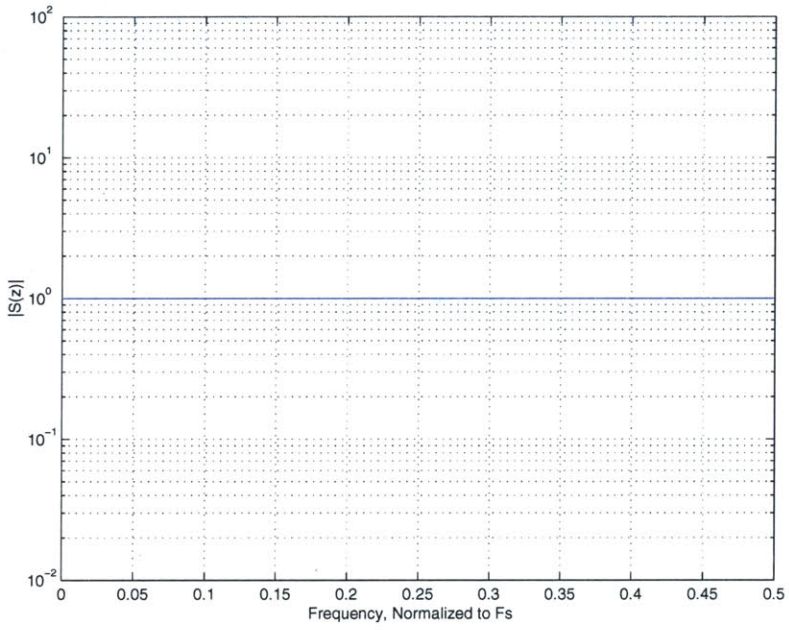

Figure 2-14: Frequency Response of Signal Transfer Function

Letting $z = e^{\frac{j2\pi f}{F_S}}$, we calculate the SNR for our converter for a sinusoidal input voltage with bandwidth f_B. After some math, we find the magnitude of the noise transfer function as a function of frequency is given by

$$|N(f)| = 2\sin\frac{\pi f}{F_S} \tag{2.11}$$

Now we find the noise power over our input frequency band $[0, f_B]$

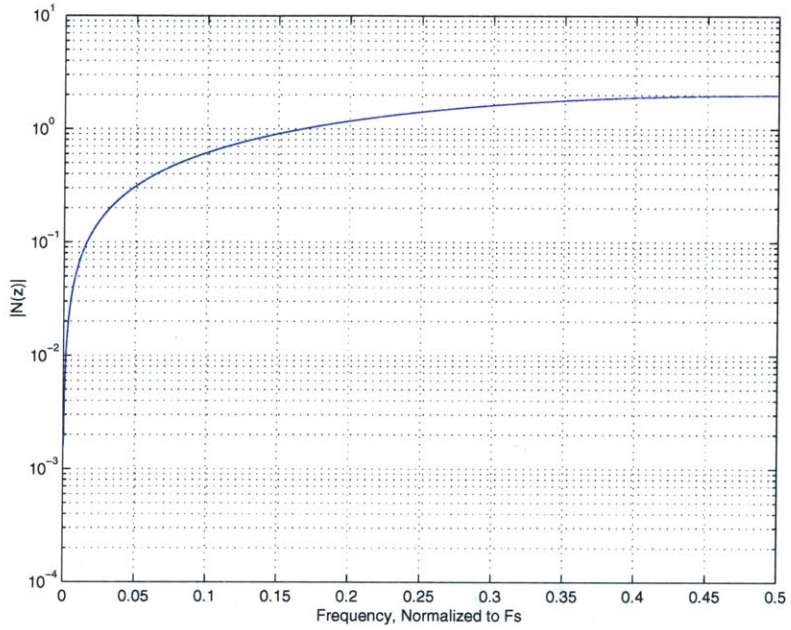

Figure 2-15: Frequency Response of Noise Transfer Function

$$P_q = \int_{-f_B}^{+f_B} (S_e(f))^2 |N(f)|^2 df = \int_{-f_B}^{+f_B} \frac{\Delta V^2}{12(\frac{DF_s}{2})} (2\sin(\frac{\pi f}{F_S}))^2 df \tag{2.12}$$

Since $D >> 1$, we may approximate $\sin(\frac{\pi f}{F_S})$ as $\frac{\pi f}{F_S}$, which yields

$$P_q = \frac{\Delta V^2 \pi^2}{36} (\frac{1}{D})^3 \tag{2.13}$$

With $P_s = \frac{(2^N)^2(\Delta V)^2}{2}$ as before, the maximum SNR for this $\Sigma\Delta$ A/D converter is given by

$$SNR = 10\log\frac{P_s}{P_q} = 6.02N + 1.76 - 5.17 + 30\log(\frac{3}{\pi^2})(D^3), \text{ where N=1.} \tag{2.14}$$

We see from Equation 2.14 that using a negative feedback loop to shape the quantization noise with a first-order high-pass function yields an SNR enhancement of $\frac{3D^3}{\pi^2}$ over that of converter's achievable SNR with oversampling alone. The 5.17dB loss that we see in Equation 2.14 stems from the the noise shaping loop. While greatly attenuating the inband quantization noise, this loop boosts the total power of the

quantization noise because it has some gain associated with it. This characteristic results in the negative term in Equation 2.14 [1].

In the previous section, we saw how oversampling alone does not allow us to achieve the high level of SNR needed for our application with a 1-bit quantizer. This was because the oversampling ratio was simply too large to make implementation feasible. To see how a $\Sigma\Delta$ A/D converter's noise shaping loop allows us to sample at a lower frequency, consider the same sinusoidal signal bandlimited to 20kHz as an input to the converter. Again, we demand 20-bit precision at the output of the converter. Using Equation 2.14, we find that required sampling rate has decreased from 8.6GHz with oversampling alone to 387.6MHz with the addition of noise shaping. We will soon see how increasing orders of high-pass noise shaping will increase the resolution payoff and further reduce the required oversampling ratio for a given SNR. And with a lower oversampling ratio we can relax the speed requirements on the components within the noise shaping loop.

2.5 $\Sigma\Delta$ Conversion - Time Domain Perspective

Our discussion of $\Sigma\Delta$ conversion to this point has been from a linearized frequency domain standpoint, now we look at these converter's operation from the time domain. Because we have oversampled our input signal, its value changes very slowly compared to the sampling frequency. Referring to Figure 2-13, except for the case when the input $x[n]$ exactly equals one of the binary values of the quantizer, a tracking error comes about ($t[n] = x[n] - y[n]$). The integrator in the forward path accumulates this error over time and the quantizer simply feeds back a value that will minimize this accumulated error such that the long-term average of this tracking error is zero. Thus, $y[n]$ can be viewed as a rapidly changing approximation to our input signal that has an average value equal to $x[n]$ [15].

2.6 Spurious Tones

Thus far, the only source of converter error that we have looked at is that due to quantization. Leveraging the time domain point of view above, we now look at another source of error present in $\Sigma\Delta$ converters– *spurious tones.* Even when utilizing ideal analog components, low-order 1-bit noise shaping loops are prone to this error which is oscillatory in nature. It is brought about by certain DC inputs that cause the quantization error to be deterministic. That is, the additive independent white noise approximation that we made for the quantization noise earlier no longer holds. For these certain inputs, the binary quantizer output $y[n]$ will exhibit a long, usually complex pattern. When the period of this sequence is long enough, its fundamental component lies in the band of our signal of interest and will not be attenuated by the decimator and thus our SNR is degraded. Even though our converter operates on an AC signal, we concern ourselves with spurious tones because, in practice, any AC signal generally has some DC component associated with it.

A simple Matlab script was written to illustrate these repetitive patterns. Consider a first-order $\Sigma\Delta$ converter with input range $[0V, 1V]$ and a 1-bit quantizer with output levels 0V and 1V. For a DC input of $\frac{1}{2}$V to the converter, we get the following quantizer output sequence: $y[n] = 1, 0, 1, 0, 1, 0, \ldots.$ This sequence has its power at DC and $\frac{F_S}{2}$. The $\frac{F_S}{2}$ component will be filtered by the decimator leaving us with only a DC component. Now let us consider a DC input level of $\frac{1}{2}$V + $\frac{1}{22}$V to our converter. This yields a quantizer output sequence $y[n] = 1, 0, 1, 0, 1, 0, 1, 0, 1, 1, 0, 1, 0, 1, 0\ldots.$ We see that this output sequence has its power at DC and at $\frac{F_S}{11}$. If our converter's OSR is equal to 5 (i.e. $f_B = \frac{F_S}{10}$, then the decimator will not eliminate the signal's power at $\frac{F_S}{11}$ and we will get a *tone* in our output spectrum in addition to the DC component.

There are a number of ways to mitigate the effect of spurious tones on the performance of $\Sigma\Delta$ converters. These methods include the addition of a random signal into the loop just before the quantizer so that the quantization noise is not deterministic. Another solution to make our AIWN approximation hold true is to use a multibit quantizer. In this solution, the added quantizer levels results in a more ran-

dom quantization error. The downside to both of these techniques is they represent a large increase in complexity to a $\Sigma\Delta$ converter [1].

2.7 Higher-Order $\Sigma\Delta$ Conversion

We turn to higher order converters (i.e. those that employ more than one integrator) to help us reduce the spurious tones present in the output spectrum of first-order $\Sigma\Delta$ converters. Each integrator in these high-order loops accumulates the error from the output and that of the integrator that precedes it. The combined action these integrators operating on the error randomizes the quantization noise [11]. Additionally, higher order modulators have the added benefit of increased noise shaping as we mention below.

Previously we showed how shaping the quantization noise by placing a quantizer in a negative feedback loop with an integrator preceding it in the forward path will attenuate inband quantization noise by 9db/Octave. Yet we demonstrated that obtaining performance on the order of 120dB with this first order loop is not easily attainable from an implementation standpoint. In the literature, various high-order $\Sigma\Delta$ architectures have been proposed that result in increasing levels of noise shaping. It has been shown that an L^{th} order, noise shaping loop improves the converter's SNR by (6L + 3) dB/Octave [1]. This characteristic of higher-order converters further reduces the necessary oversampling ratio needed for a given SNR.

Various approaches to this technique have been proposed and shown to exhibit the specified level of SNR performance for our application at Draper Laboratory. In general, we can split these methods into two categories– high-order, feedback noise shaping and multistage, low-order noise shaping. We discuss these two topologies in the following sections.

2.7.1 Single-Loop, High-Order Converters

In Figure 2-16, we show a $\Sigma\Delta$ converter that has a $\Sigma\Delta$ loop embedded within another $\Sigma\Delta$ loop [1]. With two integrators in the loop, the quantization noise frequency

response rises as a quadratic function of frequency as compared to the linear relationship that we saw for the first order converter. The higher order quantization noise shaping causes noise to be further suppressed in the baseband and to rise more sharply at higher frequencies. This feature results in the reduction of the total quantization noise power in the baseband, which yields a reduction in the oversampling ratio for a given SNR.

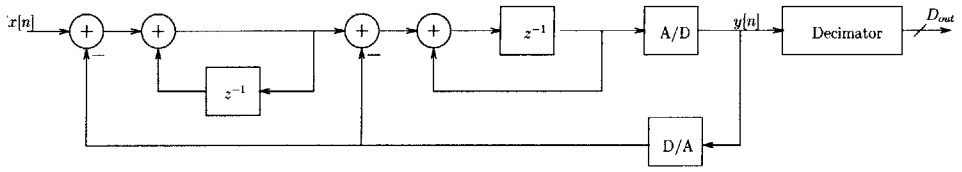

Figure 2-16: Single-Stage, Second-Order $\Sigma\Delta$ Converter Structure

Increasing the order of the noise shaping loop means that we have to consider the stability of this loop. When the loop filter, $H(z)$, contains two or more integrators, then we can expect significant phase shift at the crossover frequency leading to oscillations. However, these high-orders of noise shaping can be achieved with a more complex loop filter [5]. That is, we can design it so that it crosses over with an appropriate amount of phase margin using careful placement of poles and zeros.

A critical issue with this type of converter that still remains is that of *overload*. Overload usually occurs when the large input signals are presented to the converter. These signals cause the input to the quantizer to go beyond its normal range resulting in the quantization error becoming greater than $\pm\frac{\Delta V}{2}$. When this condition manifests, the magnitude of the loop gain is reduced and crossover at lower frequencies occurs where large phase shifts cause oscillations [1].

Due to the 1-bit quantizer in the loop, stability of single-stage, high-order converters is not well understood. In the literature, empirical analysis has provided general rules of thumb for stabilization of these higher-order loops [13]. And conditionally stable converters providing levels of SNR on the order of 130dB have been described [19], [18].

2.7.2 Multistage, High-Order Converters

To avoid the stability issue present in high-order feedback loops, a series of first- and second-order loops can be cascaded together to achieve higher orders of noise shaping. Since a multistage converter structure contains only feedforward paths and no feedback between the individual loops, it will be stable if the modulators that comprise itself are stable. This technique is shown in Figure 2-17 where two single-stage (1-1) $\Sigma\Delta$ converters have been cascaded.

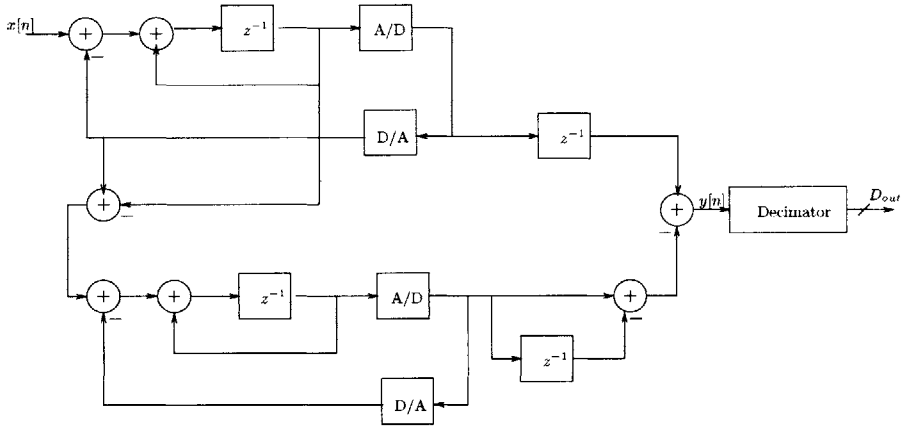

Figure 2-17: Multistage, High-Order $\Sigma\Delta$ Converter Structure

In the case of the above 1-1 cascade, the second loop operates on the quantization error residue from the first stage in the digital portion of the converter represented by the decimator in Figure 2-17. The degree of this error cancellation depends on how well the analog implementation of the loop filter matches its inverse which is represented in Figure 2-17 by the delay and and differentiator blocks. Hence, the analog performance of this multistage converter is more sensitive to the imperfections of the analog components than that of the single-loop modulator [8].

Even with a certain degree of sensitivity to analog component variations, high-order, multi-stage converters have been shown to exhibit SNR performance in the area of 120dB [14], [17]. Besides making design of the analog portion of the converter more difficult, multistage converter design does not allow us to use decimator structures that exploit 1-bit inputs [1]. Therefore, we will not be able to utilize the current

implemenation of the decimator and adding to the design process. In Chapter 1, we said that we would restrict ourselves to the decimator in place to narrow the breadth of this thesis. Thus, we do not explore this option in more depth.

Chapter 3

A Discrete-Time, Third-Order $\Sigma\Delta$ Modulator

As described in Chapter 1, Draper Laboratory presently employs a high-order, single-stage $\Sigma\Delta$ A/D converter in the contruction of high resolution MEMS inertial sensors. In this attempt to design a converter with greater accuracy, we look to aspects of the previous architecture where we might extract better performance. We focus our improvement efforts on the analog modulator portion of the $\Sigma\Delta$ converter.

This chapter serves to:

- Document the design methodology of the previous modulator's transfer function. This discussion gives us added insight on how we go about achieving high levels of quantization noise attenuation within the bandwidth of our signal.

- Investigate the circuit level implementation of this architecture. Here we observe the impact of various nonidealities such as noise, drift and process variation on the level of inband noise.

- Point to areas of weakness within this design where the figure of merit could be enhanced. And briefly discuss possible improvements to these areas and the tradeoffs that accompany them.

3.1 $\Sigma\Delta$ Transfer Function Analysis

Recall that our signal of interest is a 200Hz band about a center frequency, f_0, which is nominally 20kHz. The sampling frequency, F_S, is set to be $256 \times f_0 = 5.12$MHz. Thus, we obtain an oversampling ratio [5]:

$$D = \frac{5.12\text{MHz}}{2 \times 200\text{Hz}} = 12800 \tag{3.1}$$

Using Equation 2.7, we see that oversampling brings the quantization noise power within the band of our signal of interest to:

$$P_q = (\frac{\Delta V^2}{12})(\frac{1}{D}) = (\frac{(5V)^2}{12})(\frac{1}{12800}) = 1.63 \times 10^{-4} V^2 \tag{3.2}$$

Seeing that this results in a SNR of 43dB for a $2.5V_{pp}$ full scale input, the previous converter employs noise shaping to "push" more quantization noise power out of band.

A Matlab-based, $\Sigma\Delta$ toolbox [10] was utilized to design a noise transfer function that would attenuate the amount of inband quantization noise.[1] Figure 3-1 shows the block diagram of the previous modulator that was synthesized using this toolbox. Signal $x[n]$ is the signal to be converted. Signal $e[n]$ models the quantization noise introduced by the quantizer. And signal $y[n]$ is the output of the modulator that is to be digitally filtered.

From Figure 3-1, we determine the signal transfer function, $S(z)$, and noise transfer function, $N(z)$:

$$S(z) = \frac{(b_1c_1c_2 - b_2c_2 + b_3)z^{-3} + (b_2c_2 - 2b_3)z^{-2} + b_3z^{-1}}{(-1 + a_3 + (-a_2 - g_3)c_2 + a_1c_1c_2)z^{-3} + (3 - c_2(-g_1 - a_2) - 2a_3)z^{-2} + (-3 + a_3)z^{-1} + 1} \tag{3.3}$$

[1]The toolbox that we are referring to is "THE DELTA-SIGMA TOOLBOX Version 7.1" written by Richard Schreier of Analog Devices. Chapter 4 will contain an in depth look at usage of this toolbox.

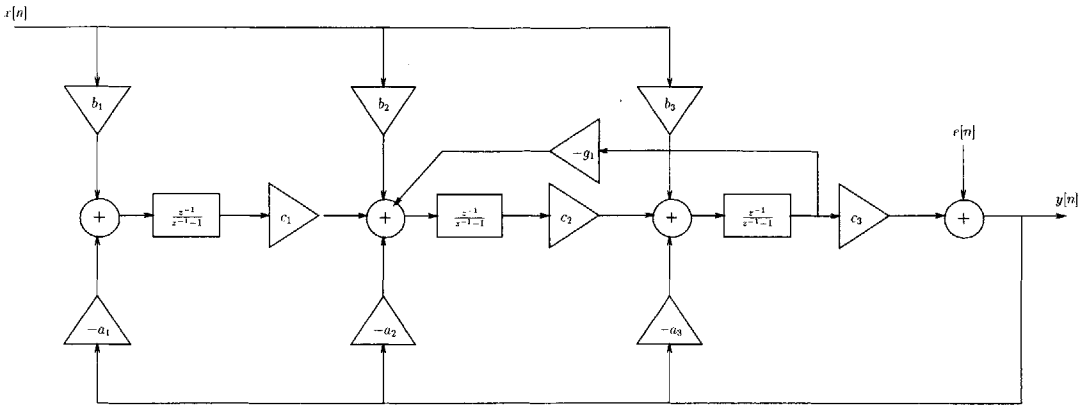

Figure 3-1: Block Diagram of 3^{rd}-Order $\Sigma\Delta$ Modulator

$$N(z) = \frac{(1-z^{-1})(1-2z^{-1}+(1+c_2g_1)z^{-2})}{(-1+a_3+(-a_2-g_1)c_2+a_1c_1c_2)z^{-3}+(3-c_2(-g_1-a_2)-2a_3)z^{-2}+(-3+a_3)z^{-1}+1} \tag{3.4}$$

Inserting the values of the constants a_i, b_i, c_i and g_i used in this design, we find that Equations 4.10 and 4.11 reduce to

$$S(z) = \frac{0.2161z^{-3}-0.5107z^{-2}+0.3125z^{-1}}{-0.7844z^{-3}+2.4898z^{-2}-2.6875z^{-1}+1} \tag{3.5}$$

$$N(z) = \frac{(1-z^{-1})(1-2z^{-1}+1.0006z^{-2})}{-0.7844z^{-3}+2.4898z^{-2}-2.6875z^{-1}+1} \tag{3.6}$$

The frequency responses of $S(z)$ and $N(z)$ are shown in Figures 3-2 and 3-3, respectively. We see the noise transfer function has a zero at DC and a complex conjugate pair of zeros at f_0. This complex pair creates a notch at f_0 that greatly supresses the amount of quantization noise power around at f_0 thereby avoiding the use of an extremely large oversampling ratio in obtaining a high SNR.

How was this notch created at f_0? A function, synthesizeNTF()[2], in the $\Sigma\Delta$ toolbox allows one to create a noise transfer function whose zeros are spread over

[2]Note: SynthesizeNTF() works like any other digital filter approximator in the Matlab Digital Signal Processing Toolbox such as or cheby1() and remez() which implement filter algorithms according to user-specified parameters like order and stopband attenuation.

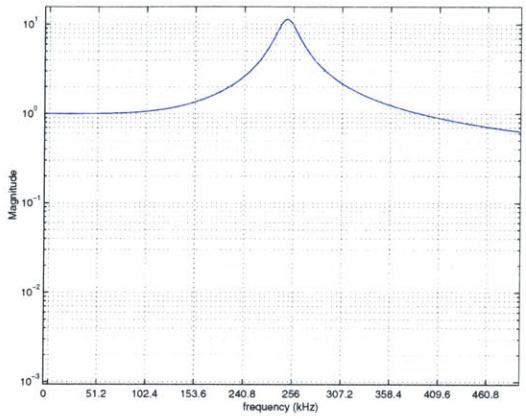

Figure 3-2: Frequency Response of the Signal Transfer Function with $F_S = 5.12$MHz

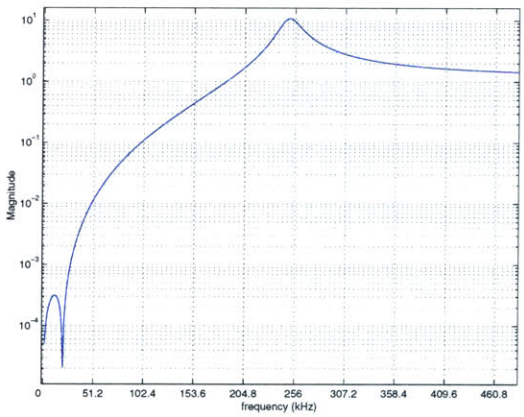

Figure 3-3: Frequency Response of the Noise Transfer Function with $F_S = 5.12$MHz

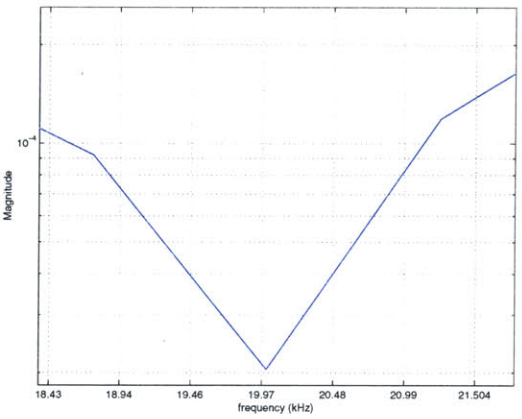

Figure 3-4: Frequency Response of the Noise Transfer Function in Area of f_0

the passband in order to more adequately shape the quantization noise. That is, instead of placing three zeros at DC for a third-order loop, one is able to spread them out evenly over some band, usually the bandwidth of the signal of interest. If the three zeros had been placed at DC, then the level of quantization noise suppression decreases as we move from DC across the band of interest. However, if the zeros are spread over the signal passband, then the magnitude of the noise transfer function over this band will remain relatively independent of frequency. In this application, the band over which the zeros are spread was varied such that the complex conjugate pair ends up at f_0. Since the signal of interest has such a small bandwidth about f_0, a high attenuation level of inband quantization noise can be attained as depicted in Figure 3-4. Using Matlab, we determine this level of attenuation to be -87dB. Given this figure, we calculate the inband quantization noise power and the modulator's SNR:

$$P_q = (\frac{\Delta V^2}{12})(\frac{1}{D})\int_{-200}^{+200Hz} |N(f)|^2 \mathrm{d}f = (\frac{(5V)^2}{12})(2\times\frac{200\mathrm{Hz}}{5.12\mathrm{MHz}})(4.54\times10^{-5})^2 = 3.35\times10^{-13} \tag{3.7}$$

$$SNR = 10\log\frac{P_s}{P_q} = 10\log\frac{\frac{(2.5V)^2}{2}}{3.35\times10^{-13}} = 130dB \tag{3.8}$$

The 134dB SNR and inband quantization noise of $41\mathrm{nV}/\sqrt{\mathrm{Hz}}$ are much different from the measured performance of the modulator. Referring to the Table 1.1, we observe that the measured results for these two values are 111dB and $140\mathrm{nV}/\sqrt{\mathrm{Hz}}$, respectively. Let us now look to a number of elements that could account for such a drastic difference in these values.

3.2 $\Sigma\Delta$ Modulator Nonidealities

Up to this point, the main source of error in $\Sigma\Delta$ converters that we have discussed is quantization noise. However as we begin to think about the actual implemenation of our converter, we find that many other error sources exist within the modulator

section. Here, we characterize a number of these sources and quantify their impact on the previous $\Sigma\Delta$ modulator's performance. In addition, we present techniques used to mitigate particular error sources which will help form some of the building blocks of the improved modulator that we present later.

3.2.1 Noise Transfer Function Imperfections

Before we introduce other sources of noise that impact our SNR, let us look at various errors within the modulator structure that impact how well we are able to attenuate inband quantization noise.

Out-of-Band NTF Gain

Noticably evident from the frequency response of the noise transfer function in Figure 3-3 is the peaking around f =256kHz. This peaking could result in signals at the quantizer input that exceed its input range. When this situation occurs, our white noise approximation for the quantization noise spectrum breaks down as the quantizer's error is no longer distributed between $[-\frac{\Delta V}{2}, +\frac{\Delta V}{2}]$. This occurrence is reflected by an increase in quantization noise power, which translates into a decreased SNR. Researchers have experimentally shown that this situation can be avoided if $|N(z)| < 2$ [15]. While this is a general rule of thumb for designing a modutor's noise transfer function, it does not have a thorough justification and it is not always a sufficient constraint [13]. At this time, simulations are the most reliable method for seeing if quantizer overload will occur in a given modulator. Often designers choose to employ additional circuitry for detecting quantizer overload and modifying the modulator such that this condition disappears.

Pole-Zero Placement Errors

In Figure 3-5, we take a close look at the frequency response of the noise transfer function in the area of f_0. We note that the notch that was created here does not occur exactly at 20kHz, nor does the magnitude drop to zero. The reason for the

second fact is that the complex conjugate pair of zeros do not lie on the unit circle. The pole zero diagram in Figure 3-5 illustrates the location of this complex conjugate pair. From the numerator in Equation 4.11, we see that the complex conjugate zeros occur at $1 \pm \sqrt{-c_2 g_1}$. Hence, we only get a pair of zeros that reside on the unit circle if $-c_1 g_1 = 0$. If $-c_2 g_1 > 0$, then these zeros lie on the real axis. And if $-c_2 g_1 < 0$, then this zero pair will be complex with real part equal to 1. As shown in Figure 3-5, the zeros of the previous modulator occur at $1 \pm 0.0245j$. Since these zeros are not on the unit circle, they cannot completely attenuate the quantization noise at their frequency. But because the displacement of this complex conjugate pair from the unit circle is so small, we do a observe a level of quantization noise attenuation that is quite large in the vicinity of f_0.

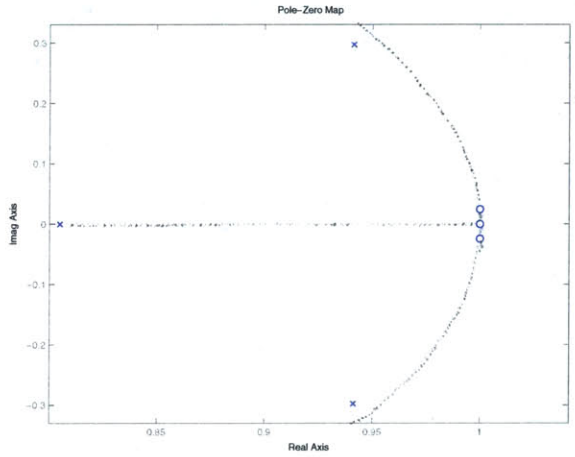

Figure 3-5: Noise Transfer Function Pole Zero Map

Let us see how we might modify the block diagram in Figure 3-1 to yield zeros that lie on the unit circle to give us more attenuation. Suppose we were to replace the second or third accumulators seen in this block diagram with a delayless integrator. Such an integrator will have a transfer function of the form $\frac{1}{1-z^{-1}}$. Finding the closed loop transfer function of the structure seen in Figure 3-6, we obtain:

$$R(z) = \frac{B}{A}(z) = \frac{c_2 z^{-1}}{1 - (2 + g_2 c_2) z^{-1} + z^{-2}} \tag{3.9}$$

The poles of $R(z)$ will map to zeros in the the noise transfer fucntion. We find the

poles to be located at $\frac{(2-c_2g_1)}{2} \pm \frac{\sqrt{(c_2g_1)^2-4c_2g_1}}{2}$. Since the system's coefficients vary between 0 and 1, we know that these poles will be complex. After some algebra, we find that distance from these complex poles to the origin is 1, thus they lie on the unit circle. Hence, we are able to get much greater attenuation of inband noise by switching to this resonator structure. Figure 3-7 illustrates how these poles move around the unit circle as the c_2g_1 product is varied. The downside with this quantization noise reducing method is that it makes the implementation of the modulator more complex by doubling the settling time requirements on the operational amplifiers within the loop [8]. We will cover more of these circuit-level implementation details in greater depth later.

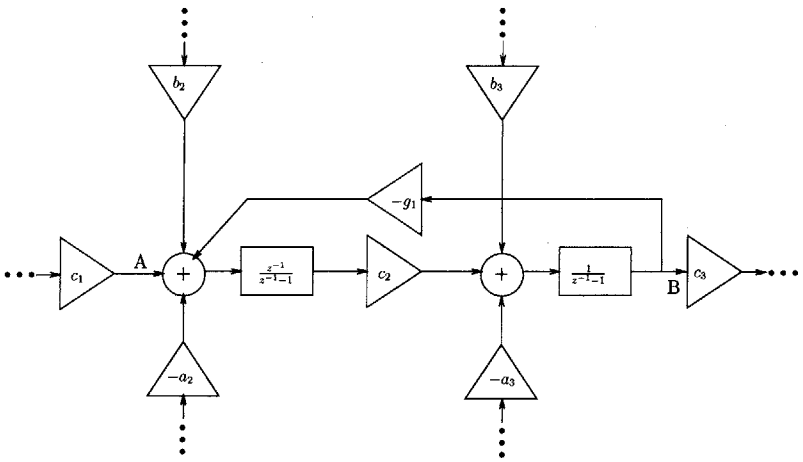

Figure 3-6: Resonator Structure that allows for Complex Conjugate Zeros along Unit Circle

Coefficient Quantization

As previously mentioned, the notch in the noise transfer function does not occur exactly at 20kHz. This placement error is due to coefficient quantization. Ideally, we can arbitrarily place the notch at 20kHz by being able to choose the c_2 and g_1 values with infinite precision. However, in practice, each coefficient (a_i, b_i, c_i, and g_i) is set by a ratio of two capacitors. Since we canot layout these capacitors with infinite precision, then we cannot just place the notch at an arbitrary 20kHz. In this

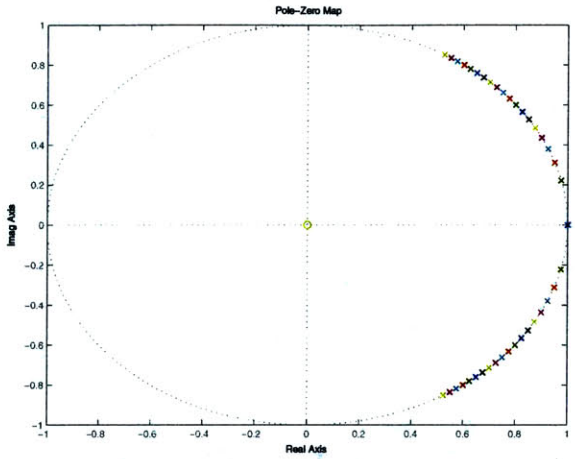

Figure 3-7: Some Possible Placements of Noise Transfer Function Complex Conjugate Zeros with Resonator Structure

3^{rd}-order modulator, coefficient quantization causes the complex conjugate zero pair to lie at 19.95kHz. It can be shown that this 50Hz difference in actual and desired notch location only results in an error of a 1 or 2dB.

Capacitor Mismatch

Yet another reason for why the notch due to the complex conjugates zeros does not lie exactly at 20kHz is capacitor mismatch. In modern integrated circuit processes, the absolute value of a capacitor can vary as much as $\pm 30\%$. However, this design exploits the fact that the ratio between two on-chip capacitors is well-controlled. That is, one can expect the mismatch between two equal capacitors to be on the order of $\pm 0.3\%$. Montecarlo simulation in Matlab has shown that the previous modulator's structure is very insensitive to capacitor mismatch. Figure 3-8 indicates that the noise transfer function magnitude varies by less than 2dB over the band of interest with variations in capacitor ratios. These plots were created by generating each coefficient with a gaussian distribution with mean equal to the coefficient value and standard deviation 0.3%.

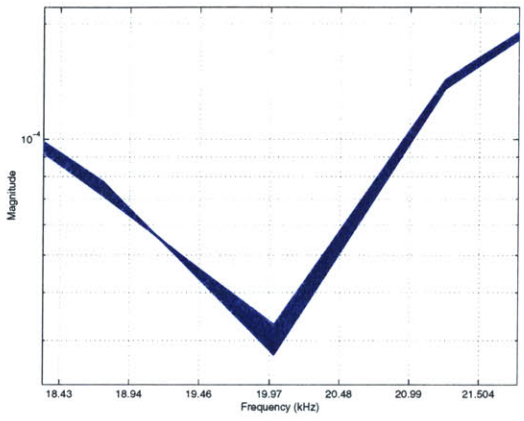

Figure 3-8: Effect of Capacitor Mismatch on the Noise Transfer Function Frequency Response in Area of f_0

Nonideal Circuit Effects on Noise Transfer Function

We have been examining how the small changes in the coefficients and structure of our modulator affect performance by altering the noise transfer function. Continuing this discussion of gain and pole/zero placement errors it is useful to mention the role of nonideal effects in the circuit-level implementation on the noise transfer function. For example, nonzero switch resistance, finite op-amp bandwidth and finite op-amp gain all shape the noise transfer function. For most single-stage modulator implementations the gain errors that results from these imperfections can be ignored in hand calculations [8]. However, as we will see in the following section, these circuit nonidealities account for the greatest source of inband noise in any $\Sigma\Delta$ modulator.

3.2.2 Contribution of Circuit Noise to SNR Degradation

The performance of a well-designed high-resolution $\Sigma\Delta$ modulator should generally be limited by the analog noise sources contained within the loop [5]. This analog noise consists of the thermal and flicker noise of the transistors that comprise the modulator. Since these noise sources determine the power dissipation and circuit size of the modulator, it is imperative to maximize their noise budget [17]. The most common approach to doing this is to reduce the modulator's inband quantization noise so that its noise contribution is negligible with respect to overall performance.

The previous point illustrates why the noise transfer function was designed to bring the inband quantization noise density down to $42\text{nV}/\sqrt{\text{Hz}}$. In Table 3.1, we list the input referred noise density that stems from the various analog noise sources within the loop.

Noise Source	**Input Referred Noise in 200Hz Bandwidth about f_0, Nominally 20kHz.**
Quantization Noise	$41\text{nV}/\sqrt{\text{Hz}}$
Sampling Noise	$40\text{nV}/\sqrt{\text{Hz}}$
Flicker Noise	$145\text{nV}/\sqrt{\text{Hz}}$
Aliased Thermal Noise	$53\text{nV}/\sqrt{\text{Hz}}$
Total	$166\text{nV}/\sqrt{\text{Hz}}$

Table 3.1: Converter Noise Sources at 20kHz

Before we detail how we came about the numbers in Table 3.1[3], it is necessary that we look at the circuit structure that we use to realize the modulator block diagram of Figure 3-1. Three switched-capacitor integrators are the main building blocks of the third-order $\Sigma\Delta$ modulator. The structure of each of these integrators is shown in Figure 3-9. The major benefit of this structure is that one sampling capacitor is needed to peform the subtraction of the error voltage ($V_{fb\pm}$) and the addition of the feedthrough input voltage which reduces the amount of sampled noise in our circuit. An explanation of the operation of this modulator's integrators can be found in the graduate thesis of Keith Santarelli [3] and in [6]. In the context of this discussion, it is only pertinent to analyze the noise contribution of this circuitry. Specifically, since the gain of the first opamp is quite large (i.e. on the order of 80dB), we can neglect the noise sources of the following integrator stages and only consider the noise of the first stage, which is shown below.

Sampling Noise

A capacitor does not generate any noise; however, it does accumulate noise from other sources. For example consider a circuit solely composed of a capacitor connected in

[3]The quantization noise is as calculated in Section 3.1. And the opamp's input referred flicker and thermal noise were obtained via HSPICE simulation.

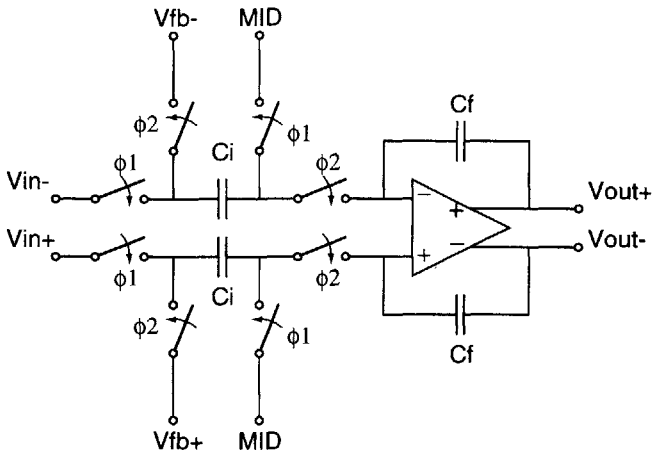

Figure 3-9: Fully-Differential Switched-Capacitor Integrator Structure used in Previous Modulator

parallel with a resistor of any size. It can be shown that the mean square value of the noise voltage that appears across the capacitor is equal to kT/C [5]. Now consider the sampling system in Figure 3-10 which operates at rate f_S. When the switch is opened, the resistor noise voltage is stored on the capacitor. If the sampling period is much longer than the RC time constant, then all the resistor noise aliases into the band $[0,f_S]$. Furthermore if the system were oversampled by a ratio D, then the noise that appears in the inband has mean squared value given by $V^2_{samp} = \frac{kT}{DC}$, where k is Boltzmann's constant 1.38×10^{-23}J/K and T is temperature in Kelvins.

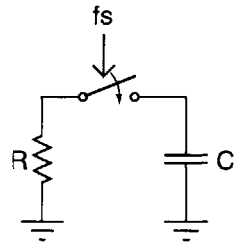

Figure 3-10: Sampled RC Circuit

Replacing the ideal switch and resistor in Figure 3-10 with a MOS transistor, we begin to apply this concept to our modulator's front-end integrator. When the MOS transistor is turned on, its channel can be considered resistive and thus it generates thermal noise. Recognizing that our front-end has two capacitors, we find

the sampling noisepower that falls into our band of interest to be [6]:

$$V_{samp}^2 = \frac{2kT}{DC} = \frac{2 \times 1.38 \times 10^{-23} J/K \times 300K}{12800 \times 2pF} = 3.2 \times 10^{-15} V^2 \tag{3.10}$$

Clearly evident from the above equation is that our sole degree of freedom in changing the amount of sampling noise present in this modulator is through changing the capacitor size. Since many high-resolution $\Sigma\Delta$ modulators are dominated by capacitor area, then it wise to ensure that this sampling noise dominates all the rest of the noise sources in the circuit by a large margin [8]. Restricting ourselves to the use of 2pF sampling capacitors, we have established the noise floor of our improved modulator to be $40\text{nV}/\sqrt{\text{Hz}}$. Thus we must focus our efforts in our improved modulator in keeping the inband noise contributions of the other noise sources in the modulator well below this level. With this design point in mind, we already know that one of our tasks will be to decrease the amount of inband quantization noise as we observed its value to be $40\text{nV}/\sqrt{\text{Hz}}$. Let us now look to the two remaining sources of inband noise that we must take into account in our improved modulator.

Opamp Thermal Noise

We model the thermal noise of the opamp in our front-end integrator as a voltage source at the gate of each transistor in the opamp's input differential pair. This gate referred thermal noise density for a MOS transistor is white and is equal to $\frac{8kT}{3g_m\Delta f}$, where g_m is the transistor's transconductance. If we ensure that the thermal noise of our opamp is dominated by its input differential pair, then the spectral density becomes approximately $\frac{16kT}{3g_m}$. Given that this noise is broadband and the sampling nature of the integrator, the thermal noise that is normally above our band of interest gets aliased back into this band. The input referred opamp inband thermal noise power is then given by the relation:

$$V_{th}^2 = (\frac{16kT}{3g_m})(\frac{f_c}{D}) = (12.6nV/\sqrt{\text{Hz}})(\frac{45MHz}{12800}) = 53nV/\sqrt{\text{Hz}} \tag{3.11}$$

where f_c is the noise bandwidth of our circuit, which is equal to the opamp's unity gain frequency in our integrator configuration. Thus we must make certain that our broadband opamp noise is minimized by careful choice of g_m and the unity gain frequency for our improved modulator.

Opamp Flicker Noise

The other noise source in our opamp is flicker noise, which is also known as 1/f noise because it has a spectral density that is inversely proportional to frequency. It is caused by imperfections within the gate oxide that capture and release carriers with a range of time constants. The spectral density of flicker noise which is modeled as a voltage source in series with the gate is given by the relation [7]

$$V_f^2 = \frac{K}{WLC_{ox}} \tag{3.12}$$

where K is a process dependent parameter. W and L are the transistor's width and length. C_{ox} is the gate capacitance per unit area [5]. Since the flicker noise power falls with frequency, the aliasing effect that we saw with thermal noise at multiples of the sampling frequency has a negligible impact on our inband noise power.

As seen in Table 3.1, flicker noise is the dominant analog noise source in this modulator. As the input referred flicker noise of a $\Sigma\Delta$ modulator is approximately equal to the input referred flicker noise of the opamp in the first integrator, we can substantially reduce its value by utilizing larger devices in the input differential pair of the opamp. However, this solution can result in substantial area increases which may not be permissible in a given application. Moreover, large input transistors can degrade the settling performance due to the opamp having increased input capacitance [6].

Correlated double sampling (CDS) is another technique for low frequency noise reduction in $\Sigma\Delta$ modulators. With this technique the signal charge transfer from input to output is made nearly independent of the opamp's offset voltage. This is accompished by introducing a zero at DC in the opamp offset voltage's transfer

function to the output. And since the flicker noise power is concentrated at low frequences, CDS reduces this noise to a negligible level. The disadvantage to CDS is that it increases the complexity of our integrator by the addition of extra switches and capacitors. These extra components can also lead to an increased amount of kT/C noise.

3.3 The Path to an Improved $\Sigma\Delta$ Modulator

As outlined in Chapter 1, our goal is to design a modulator with increased SNR performance. We now set out to accomplish this task by reducing the amount of inband noise, which we said should be dominated by the kT/C noise of the sampling capacitors in the first integrator. In the next chapter, we design a new modulator noise transfer function that serves to make the amount of inband quantization noise negligible with respect to the sampling noise. And in Chapter 5, we propose a new integrator structure that highly attenuates the amount of inband noise due to the flicker noise of the opamp, which we saw as being the limiting factor in the SNR performance of the previous modulator.

Chapter 4

Transfer Function Design for a Fourth-Order, Discrete-Time, Bandpass $\Sigma\Delta$ Modulator

Our goal is to design a $\Sigma\Delta$ modulator that achieves greater performance than the third-order modulator presented in Chapter 3. In particular, we require the input referred noise noise density be lower than $40\text{nV}/\sqrt{\text{Hz}}$ in a 200Hz region about f_0 and that the input range be 5V_{pp}. As we pointed out in the last chapter, in successful $\Sigma\Delta$ modulator design it is critical that the noise due to the analog circuit componentry be the dominant source of noise within the band of interest.

This chapter details the design of a fourth-order loop-filter that is able to shape the quantization noise at the modulator output such that its inband contribution is on the order of $0.4\text{nV}/\sqrt{\text{Hz}}$ which is neglible compared to the circuit's noise floor that is set by the kT/C noise. We start by presenting a number of high-level choices that one is forced to make in designing any $\Sigma\Delta$ modulator. This discussion illustrates why we chose the characteristics of our modulator to be fourth-order, bandpass and discrete-time. Then we synthesize our loop filter and demonstrate that it achieves the desired level of performance.

4.1 Design Choices

4.1.1 Continuous-Time verses Discrete-Time

The most common first step in the design of any $\Sigma\Delta$ modulator is choosing whether it will be implemented in continuous-time (CT) or discrete-time (DT). The decision between these two topologies hinges on whether the given application is better suited for an active-RC or switched-capacitor (SC) realization. The previous chapter described the construction and performance of a DT loop, so let us take a moment to illustrate the benefits and tradeoffs that we encounter if we were to move a CT modulator.

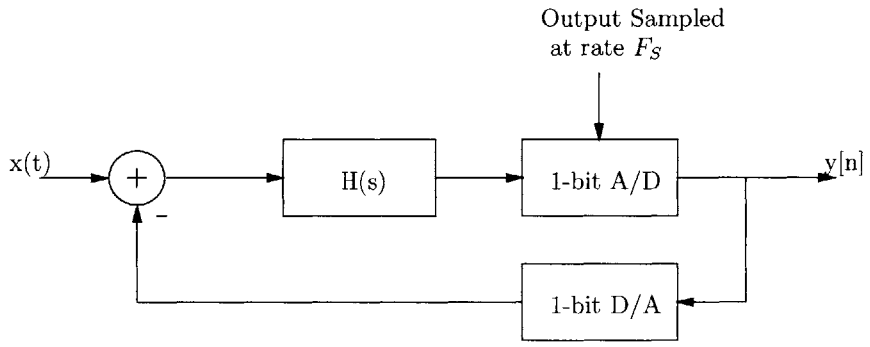

Figure 4-1: A Generalized CT $\Sigma\Delta$ Modulator

The majority of $\Sigma\Delta$ modulators in the literature have been implemented in CMOS technology as SC networks. These SC circuits can be easily realized from z-domain transfer functions, which encapsulate the behavior of a sampling system. However, opamp settling time requirements restrict sample rates of discrete-time SC modulator implementations to one-half or less of the unity-gain bandwidth of its operational amplifiers. Thus SC modulators have not achieved the maximum clock rates available in current CMOS technoology. Conversely, CT modulators have been shown to run at higher sampling rates than their SC counterparts as the opamp integrators within the noise shaping loop are not subject to settling time requirements. This feature of a CT $\Sigma\Delta$ modulator allows one to operate at higher oversampling ratios for a given input signal bandwidth [8].

Since our sample rate is set at $256 \times f_0$ ($= 5.12$MHz), we can easily meet the opamp settling time requirements in a DT loop. So why should we still consider constructing a CT $\Sigma\Delta$ modulator? Because in a number of applications CT modulators have been shown to consume less area and power than DT versions that achieve relatively the same SNR performance. These two results stem from the facts that CT $\Sigma\Delta$ structures require fewer capacitors and have opamps whose bandwidth requirements are relaxed.

Unfortunately, the drawbacks that accompany these reductions in chip area and power can be very significant. As shown in the CT integrator in Figure 4-2, the pole and zero locations are determined by an RC product verses a capacitor ratio in SC circuits, which is well controlled. Accurate RC time constants are not possible in integrated designs due to process tolerances which can results in errors in the absolute value of resistor or capacitor size in the neighborhood of 25%. Errors in these time constants restrict our ability in realizing the desired noise transfer function.

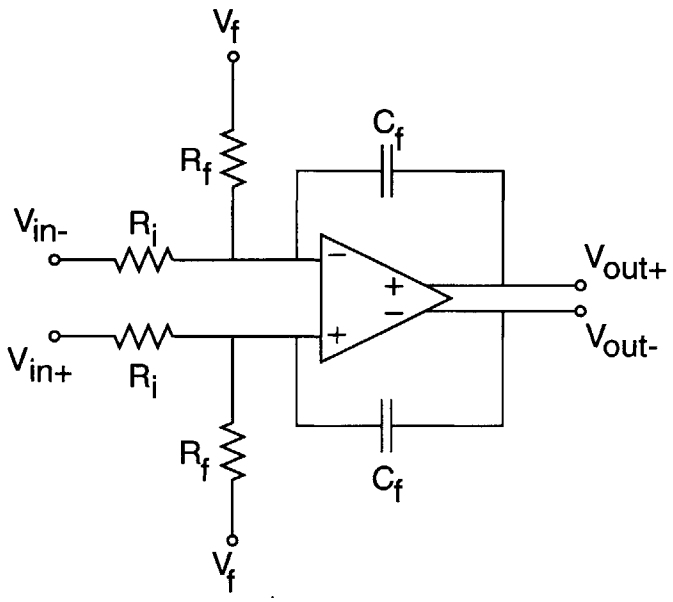

Figure 4-2: Fully-Differential CT Integrator that was used in the $\Sigma\Delta$ Modulator seen in [2]

Additionally, CT $\Sigma\Delta$ modulators are more sensitive to clock jitter than DT designs. This increased susceptibility arises in a CT design because the feedback waveform is a pulse of a current that sets a voltage across a feedback resistor compared to

an exponentially decaying pulse of current that sets the voltage across the feedback capacitor in a DT system. Therefore, for equal clock variations, the error energy that is fed back in a CT system is much larger resulting in a greater amount of input referred noise[1]. This SNR degradation due to clock jitter is the most prohibitive factor in moving to CT $\Sigma\Delta$ modulator implementations [8]. This point is best illustrated in [2].

The feasibility of a CT $\Sigma\Delta$ modulator for our application was explored by the graduate thesis work of Philip Juang [2]. Juang designed, fabricated and tested 3^{rd}- and 4^{th}-order CT modulators with MOSIS's .5μm CMOS process- the process that our modulator design is based on. The results of this previous work indicated that designing an integrated CT modulator for this application that is robust against temperature effects and process variations would be very difficult. This conclusion reinforces what we have seen in the literature where CT $\Sigma\Delta$ modulators are utilized in high-frequency applications where SNR performance on the order of 60 to 80dB is needed. In recent work, CT modulators capable of 100dB performance have been demonstrated; however, this figure is still too low for us to make further CT modulator research justifiable. Thus, we elect to implement our modulator in discrete-time where modulators that achieve SNRs in the area of 140dB have been developed over the past decade [18], [21].

4.1.2 Loop Order Selection

With our choice of a DT implementation and a set sampling rate of $256 \times f_0$, we seek to employ a high-order loop filter $H(z)$ in order to attenuate the quantization noise power in a 200Hz band centered about f_0 (nominally 20kHz).

For illustrative purposes let us consider an input signal to our modulator that is in the band from DC to 200Hz. We construct a series of noise transfer functions with increasing loop order, L, using Schreier's Matlab Delta-Sigma Toolbox[2]. All the noise

[1]We define the error energy to be the area of the voltage times current feedback waveform over a time interval that represents the clock variation.

[2]This toolbox is widely used in the development of $\Sigma\Delta$ modulators and should be utilized early on in the design process. [12]

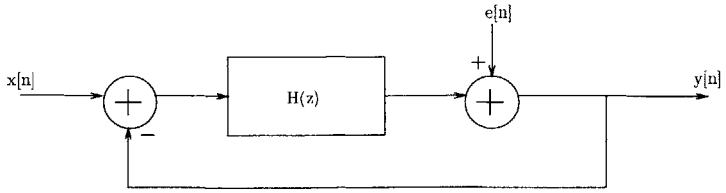

Figure 4-3: Linearized ΣΔ Modulator Block Diagram

transfer function zeros occur at DC. Hence, the numerator of $N(z)$ is $(1-z^{-1})^L$. The toolbox function (synthesizeNTF()) that we utilize to create our noise transfer functions maps the poles to locations such that the magnitude of the out-of-band noise transfer function gain is kept below 1.5 (i.e. $N(z) < 1.5$ for all z). We briefly discussed why this is a necessary constraint in Chapter 3. The four different noise transfer functions that we generated are listed in Table 4.1.

Loop Order, L	$N(z)$
1	$\frac{(z-1)}{(z-0.3333)}$
2	$\frac{(z-1)^2}{(z^2-1.225z+0.4415)}$
3	$\frac{(z-1)^3}{(z-0.6694)(z^2-1.531z+0.6639)}$
4	$\frac{(z-1)^4}{(z^2-1.493z+0.5647)(z^2-1.702z+0.7871)}$

Table 4.1: Modulator Noise Transfer Functions with Coincident Zeros at DC

The full-scale SNR performance of each modulator noise transfer function is predicted by Equation 4.1 which we have seen before in Chapter 3.

$$SNR = 10\log\frac{P_s}{P_q} \tag{4.1}$$

where P_s is given by

$$P_s = \frac{(V_{FS})^2}{2} = \frac{(2.5)^2}{2} = 3.125V^2 \tag{4.2}$$

and where P_q is given by

$$P_q = (\frac{\Delta V^2}{12})(\frac{1}{D})\int_{-200\text{Hz}}^{+200\text{Hz}} |N(f)|^2 \text{d}f = (\frac{(5V)^2}{12})(2\times\frac{200\text{Hz}}{5.12\text{MHz}})(|N(f)|^2) \tag{4.3}$$

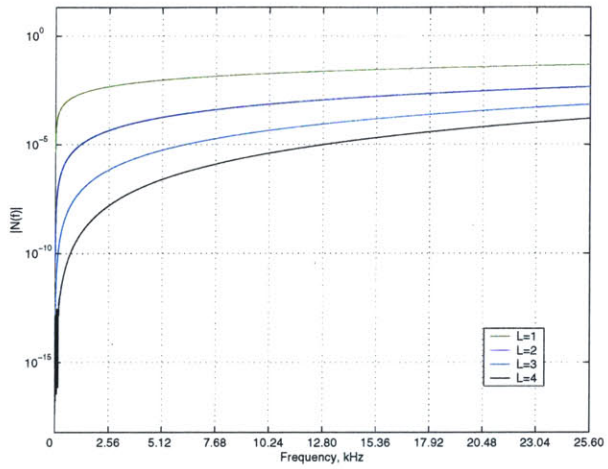

Figure 4-4: Noise Transfer Function Frequency Reponse for Coincident Zeros at DC

Note that $N(f)$ changes depending on the order of the loop filter. We show the SNR performance that each modulator noise transfer function in Table 4.1 achieves in Table 4.2.[3]

Loop Order, L	**Full Scale SNR**
1	111dB
2	174dB
3	232dB
4	287dB

Table 4.2: Theoretical Modulator SNR for NTF Coincident Zeros at DC and Input Signal Band 0 to 200Hz

Looking at the SNR characteristics for the different loop filters, we see that a second order modulator attenuates the inband quantization noise power enough to allow one to achieve a full scale SNR of about 175dB, which means that the quantization noise density is well below the circuit's noise floor. However, our signal of interest is not contained in the band DC to 200Hz; rather, it is in this same bandwidth about 20kHz! Table 4.3 lists each loop filter's SNR in this range.

Readily apparent in Table 4.3 is a large decrease in SNR performance from the hypothetical case of our signal band being located between DC and 200Hz. This fall

[3] $|N(f)|^2$ was calculated by taking the square of the output of the function rmsGain() in the Matlab toolbox. rmsGain() computes the root mean-square gain of a given discrete-time transfer function over some frequency band of interest.

Loop Order, L	Full Scale SNR
1	71dB
2	94dB
3	112dB
4	127dB

Table 4.3: Theoretical Modulator SNR for NTF Coincident Zeros at DC and Input Signal that is a 200Hz Band about 20kHz

in SNR was simply the result of the quantization noise response exhibiting a high-pass characteristic and thus having a gain that increases with frequency. One option for accounting for this fact is to spread the zeros out over the band of interest. For instance, if our input signal occupied the audio band, then we would want to spread the zeros from DC to 20kHz. This would keep the quantization noise attenuation relatively independent of frequency over the band of interest. Since our modulator's input signal is at 20kHz, we utilize the synthesizeNTF() function to create noise transfer functions of order 1 to 4 with optimized zeros over the 20kHz band. That is, we get quantization noise attenuation at 20kHz that is on the same order of magnitude as that at lower frequencies. SynthesizeNTF() accomplishes this by placing the zeros such that the RMS noise transfer function gain is minimized over the band of interest. Table 4.4 lists the transfer functions that we created whose frequency response is shown in Figure 4.5.

From Table 4.5, we see that a fourth order loop filter with optimized zeros gives us an SNR of 143dB. Recalling that the previous modulator's noise transfer function resulted in an SNR of 130dB, we see that our SNR has improved by 13dB and thus the quantization noise density has been reduced by a factor of 4. Keeping in mind that our modulator's noise floor is set by the kT/C sampling noise ($40\text{nV}/\sqrt{\text{Hz}}$), we see that quantization noise power still comprises almost ten percent of the total noise budget. Additionally, we saw in Chapter 3 how noise transfer function nonidealities can increase this percentage even further.

What we really desire is a loop filter that achieves performance similar to that seen in the high-order filters of Table 4.2 only in a band that is around 20kHz. That is saying we want our noise transfer function zeros to occur out at 20kHz. We can realize

Loop Order, L	$N(z)$
1	$\frac{(z-1)}{(z-0.3333)}$
2	$\frac{(z^2-2z+1)}{(z^2-1.225z+0.4415)}$
3	$\frac{(z-1)(z^2-2z+1)}{(z-0.6693)(z^2-1.531z+0.6638)}$
4	$\frac{(z^2-2z+1)(z^2-2z+1)}{(z^2-1.492z+0.5646)(z^2-1.702z+0.787)}$

Table 4.4: Noise Transfer Functions with Optimized Zeros in Band from DC to 20kHz

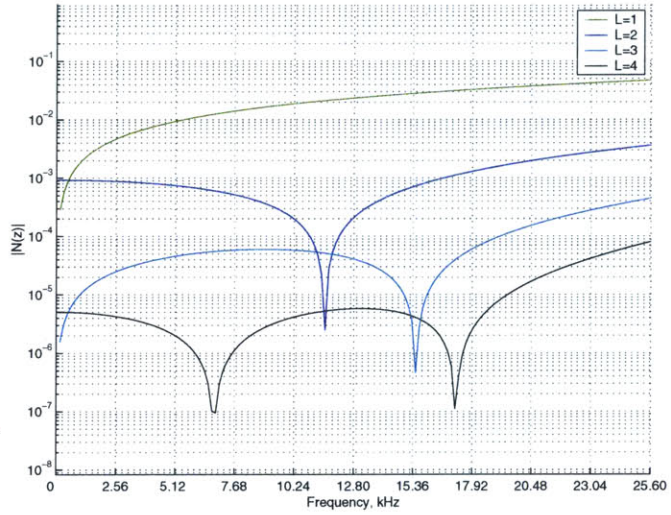

Figure 4-5: Noise Transfer Function Frequency Response for Optimized Zeros in Band from DC to 20kHz

Loop Order, L	Full Scale SNR
1	75dB
2	101dB
3	124dB
4	143dB

Table 4.5: Theoretical Modulator SNR for NTF Optimized Zeros and Input Signal that is a 200Hz Band about 20kHz

this type of noise transfer function using a bandpass filter. A bandpass filter of order L has $\frac{L}{2}$ zeros at some center frequency f_0 (f_0= 20kHz in our application). Hence a bandpass modulator of order L with coincident zeros at f_0 will achieve roughly the same SNR performance as a $\frac{L}{2}$ order modulator whose zeros are at DC [8]. Figure 4-6 shows a plot of two bandpass noise transfer functions where we locate our band's center frequency at $\frac{f_s}{256}$ (= 20kHz) and spread the zeros across the 200Hz band of interest to reduce the inband quantization noise power. As before, the noise transfer functions were created using synthesizeNTF() which we list in Table 4.6.

Loop Order, L	$N(z)$
2	$\frac{(z^2 - 1.999z + 1)}{(z^2 - 1.225z + 0.4415)}$
4	$\frac{(z^2 - 1.99941z + 1)(z^2 - 1.99938z + 1)}{(z^2 - 1.492z + 0.5647)(z^2 - 1.701z + 0.7871)}$

Table 4.6: Bandpass Modulator Noise Transfer Functions

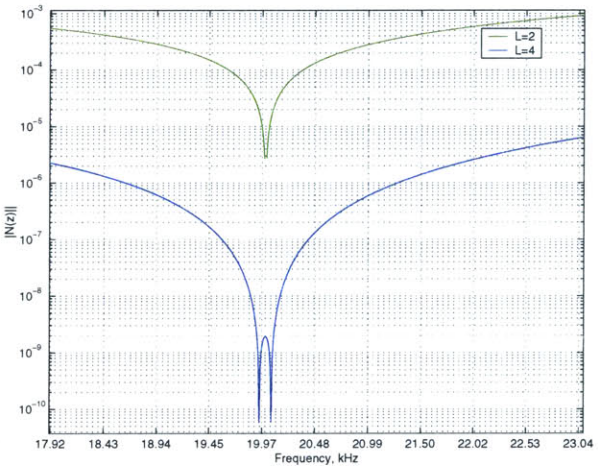

Figure 4-6: Bandpass Noise Transfer Function Frequency Response

Loop Order, L	**Full Scale SNR**
2	149dB
4	228dB

Table 4.7: Theoretical Bandpass Modulator SNR for Input Signal that is a 200Hz Band about 20kHz

Table 4.7 shows major improvements in modulator SNR over the previous noise transfer functions that we have seen for our signal of interest. Even though a second order bandpass modulator appears to be suitable in our application, we elect to employ a fourth order bandpass filter. This choice is a result of a need to widen our band of interest beyond 200Hz in order to allow for noise transfer function nonidealities which we explored in Chapter 3. As we increase the width of the notch, we get less and less inband attenuation. This dependency is shown in Figure 4-7 and Table 4.8 for a fourth order modulator. Looking at the SNR performances of the different loop filters, we see that any of the notch widths are suitable for our application as all achieve SNR performance in the area of 200dB. This figure equates to a inband quantization noise density of $0.02\text{nV}/\sqrt{\text{Hz}}$, which is well below our circuit's noise floor. We decide to make the noise transfer function notch bandwidth 800Hz as this allows for almost a $\pm 4\%$ variation in the noise transfer function center frequency relative to f_0 without performance degradation. Small changes in the notch's center frequency relative to f_0 can result from the noise transfer nonidealities that we saw in Chapter 3.

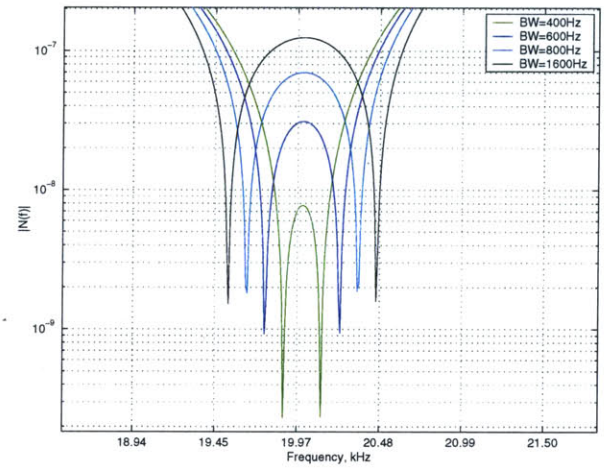

Figure 4-7: Fourth Order Bandpass Noise Transfer Function Frequency Response with Varying Notch Width

Notch Bandwidth	Full Scale SNR
200Hz	228dB
400Hz	207dB
600Hz	193dB
800Hz	186dB
1600Hz	181dB

Table 4.8: Fourth Order Bandpass Modulator SNR Variation with Input Signal Bandwidth

4.2 Loop Synthesis

Now that we have obtained our loop's noise transfer function–

$$N(z) = \frac{(z^2 - 1.99941z + 1)(z^2 - 1.99938z + 1)}{(z^2 - 1.492z + 0.5647)(z^2 - 1.701z + 0.7871)} \tag{4.4}$$

we must put it into a form that is realizable with switched-capacitor circuitry. Furthermore, we must also create a signal transfer function from the modulator's input to output. Chapter 2 gave the following relations for the signal transfer function and the noise transfer function

$$S(z) = \frac{H(z)}{1 + H(z)} \tag{4.5}$$

$$N(z) = \frac{1}{1 + H(z)} \tag{4.6}$$

As we observe from the above equations, the poles of $H(z)$ are the zeros in our noise transfer function. Also, the signal transfer function shares the same poles with the noise transfer function. These poles are given by the roots to the equation $1 + H(z) = 0$. Right now it might seem apparent that there are no degrees of freedom to independently specify the signal transfer function. However, Chapter 3 showed one possible way of doing so. The previous modulator implemented the signal and noise transfer functions with a cascade of integators with each having feedback and feedthrough inputs. These feedthrough inputs allow for independent specification of the two different transfer functions. The pair of relations for $S(z)$ and $N(z)$ change to

$$S(z) = \frac{H_0(z)}{1 + H(z)} \tag{4.7}$$

$$N(z) = \frac{1}{1 + H(z)} \tag{4.8}$$

where $H_0(z)$ is our handle for shaping the response of our signal transfer function. Its value is simply the sum of the feedforward paths from $x[n]$ to $y[n]$ and can be seen in Equation 4.10 as the numerator. This signal transfer function is designed so that it is unity over the band of interest.

One weakness of the structure that was used to realize the previous modulator was that it did not allow for placement of zeros on the unit circle. In the case of our fourth order bandpass modulator, it is of absolute importance that we be able to place zeros along the unit circle in order to achieve high levels of attenuation within the notch. In Chapter 3, we showed how using a resonator structure within the loop allowed for this zero placement on the unit circle. With this detail in mind, we add another integrator to our chain of integrators in the previous modulator and create two resonator structures within the loop to achieve two complex pairs of zero along the unit circle. Figure 4-8 shows the structure that we employ to realize our fourth order, bandpass modulator.

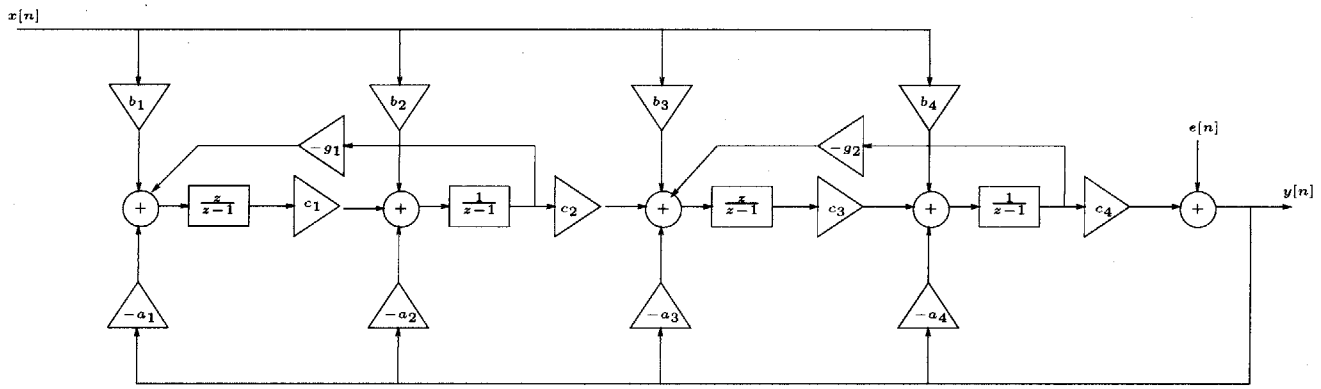

Figure 4-8: Fourth Order Bandpass Modulator Structure

After some block diagram manipulation, we can write the loop filter transfer function as

$$H(z) = \frac{\left(-a_3c_3c_4 - a_4c_4\right)z^3}{\left((z-1)^2 + c_3g_2z\right)\left((z-1)^2 + c_1g_1\right)}$$

$$+\frac{\left(2a_3c_3c_4+a_3c_1c_3c_4g_1+a_4c_1c_4g_1-a_1c_1c_2c_3c_4-a_2c_2c_3c_4+3a_4c_4\right)z^2}{\left((z-1)^2+c_3g_2z\right)\left((z-1)^2+c_1g_1\right)}$$
$$+\frac{\left(a_2c_2c_3c_4+a_4c_1c_4g_1-a_3c_3c_4-3a_4c_4\right)z}{\left((z-1)^2+c_3g_2z\right)\left((z-1)^2+c_1g_1\right)}$$
$$+\frac{a_4c_4}{\left((z-1)^2+c_3g_2z\right)\left((z-1)^2+c_1g_1\right)} \tag{4.9}$$

It follows that we get signal transfer function

$$\begin{aligned} S(z) &= b_1\frac{\left(\frac{c_1c_2z}{(z-1)^2+c_1g_1z}\right)\left(\frac{c_3c_4z}{(z-1)^2+c_3g_2z}\right)}{1+H(z)} \\ &+ b_2\frac{\left(\frac{c_2(z-1)}{(z-1)^2+c_1g_1z}\right)\left(\frac{c_3c_4z}{(z-1)^2+c_3g_2z}\right)}{1+H(z)} \\ &+ b_3\frac{\left(\frac{c_3c_4z}{(z-1)^2+c_3g_2z}\right)}{1+H(z)} \\ &+ b_4\frac{\left(\frac{c_4(z-1)}{(z-1)^2+c_3g_2z}\right)}{1+H(z)} \end{aligned} \tag{4.10}$$

and the corresponding noise transfer function

$$N(z)=\frac{1}{1+H(z)} \tag{4.11}$$

Now that we see each transfer function's dependence on the coefficients, let us begin to derive their values. As we said before, the poles of $H(z)$ are the zeros of the noise transfer function $N(z)$. Hence the noise transfer function zeros are given by the roots of the Equations 4.12 and 4.13

$$(z-1)^2+c_1g_1z=0 \tag{4.12}$$

$$(z-1)^2+c_3g_2z=0 \tag{4.13}$$

For our fourth order modulator which we listed at the end of the last section, we

have zeros located at $9.997057 \times 10^{-1} \pm j2.4257907 \times 10^{-2}$ and $9.996928 \times 10^{-1} \pm j2.482455 \times 10^{-2}$. We look to find values for the c_i and g_i coefficients. With each equation having two unknowns, we arbitrarily set each c_i coefficient equal to one and solve for g_1 and g_2. We determine g_1 and g_2 to be 5.885×10^{-4} and 6.163×10^{-4}.

As we mentioned before, the function synthesizeNTF() that we created our noise transfer function places the poles of the noise transfer function such that the out-of-band gain is kept below 1.5. Thus the a_i coefficients in the denominator of the noise transfer function are set so that this condition is met. And we have $a_1 = 6.07 \times 10^{-3}$, $a_2 = 5.25 \times 10^{-2}$, $a_3 = 2.50 \times 10^{-1}$ and $a_4 = 5.55 \times 10^{-1}$. We use the toolbox function realizeNTF() in order to find these values. realizeNTF() also finds the b_i coefficients for us ($b_1 = 6.07 \times 10^{-3}$, $b_2 = 5.25 \times 10^{-2}$, $b_3 = 2.50 \times 10^{-1}$ and $b_4 = 5.55 \times 10^{-1}$). The value of these coefficients sets the locations of the signal transfer function's feedthrough zeros. These are usually placed to cancel the roots of the characteristic equation $1+H(z) = 0$, which would result in a signal transfer function with a gain of 1 over all frequencies. Often in $\Sigma\Delta$ modulators, we can reduce the size and complexity of our circuit if we eliminate one or more of the b_i coefficients while still achieving a signal transfer function that is flat with respect to the overall converter's accuracy. Iterating in Matlab and inspecting the signal transfer function's frequency response, we find that each b_i coefficient is necessary in our application. After utilizing the toolbox to scale the coefficients to maximize our modulator's dynamic range, we get the final coefficient values[4]:

$$
\begin{array}{llll}
a_1 = .393 & b_1 = .393 & c_1 = .090 & g_1 = .0065 \\
a_2 = .306 & b_2 = .306 & c_2 = .239 & g_2 = .0013 \\
a_3 = .348 & b_3 = .348 & c_3 = .492 & \\
a_4 = .381 & b_4 = .381 & c_4 = 1.459 &
\end{array}
$$

[4]The Delta-Sigma Toolbox's scaleABCD() function will accomplish this scaling for us. This coefficient scaling is ubiquitous in switched-capacitor circuits as it has been found that switched-capacitor filters that are realized by chaining opamp integrators together achieve maximum dynamic range when all the opamp integrator outputs have the same peak amplitude [12]

Plugging the values above into Equations 4.10 and 4.11 yields the following signal and noise transfer functions whose frequency responses are shown in Figures 4-9 and 4-10, respectively.

$$S(z) = \frac{z^4 - 3.193z^3 + 3.892z^2 - 2.135z + 0.445}{z^4 - 3.193z^3 + 3.892z^2 - 2.135z + 0.445} \tag{4.14}$$

$$N(z) = \frac{z^4 - 3.999z^3 + 5.998z^2 - 3.999z + 1}{z^4 - 3.193z^3 + 3.892z^2 - 2.135z + 0.445} \tag{4.15}$$

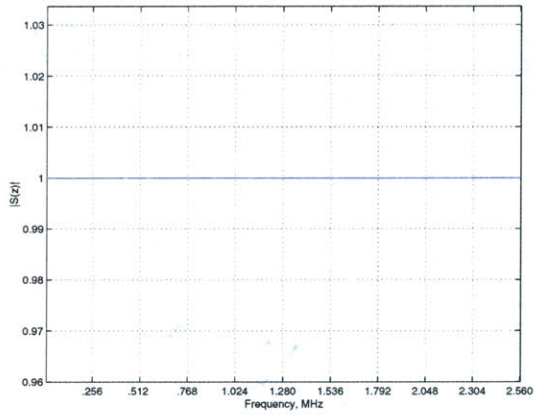

Figure 4-9: S(z) Frequency Response with Coefficients Scaled for Maximum Dynamic Range

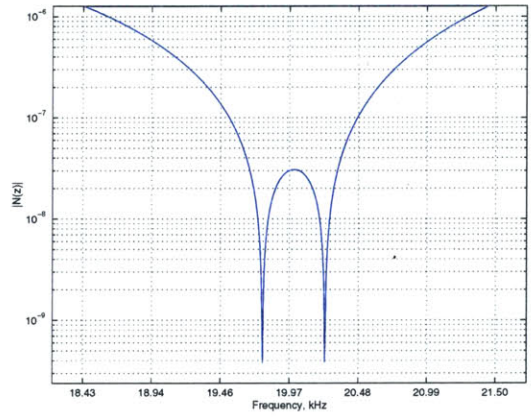

Figure 4-10: N(z) Frequency Response with Coefficients Scaled for Maximum Dynamic Range

4.3 Coefficient (Capacitor) Mismatch

As in Chapter 3, the modulator's coefficients were varied according to a gaussian distribution with mean equal to the ideal coefficient value and standard deviation equal to 0.3% in order to examine our modulator's robustness against process errors. The results of these simulations shown in Figures 4-11 and 4-12 for the noise transfer function and the signal transfer function. We see that coefficient mismatch impacts the signal transfer function in the form of a gain error over our band of interest which will not impact our converter's accuracy. However, comparing the noise transfer function of Figure 4-11 to Figure 4-10 on the previous page, we see that our inband noise attenuation shifts by almost 5dB. Yet, our modulators SNR performance is not affected as the quantization noise still remains much below the modulator's noise floor.

4.4 Modulator Performance Summary

Thus far our analysis of our new modulator has been from a linearized frequency domain standpoint. However, as we saw in our discussion of spurious tones in Chapter 2, it is critical to examine our modulator's performance from the time domain as well. We do this because the feedback loop in Figure 4-8 is described *exactly* in the time domain by a nonlinear set of difference equations which take on the form:

$$y(n+1) = f(h(n) * [x(n) - y(n)]) \tag{4.16}$$

where $h(n)$ is the impulse response of the loop filter [1]. To simplify this analysis, we turn to Matlab's Simulink and graphically construct our system. Performing time domain analysis in this environment allows to check our output spectrum for spurious tones and to find our converters maximum stable input limit. Iterating in Simulink, we find our maximum stable input range to be $2.5V_{pp}$. Note that since a fully-differential topology is used in the actual circuit implementation, the maximum stable input range should be about $5V_{pp}$ giving us an additional 6dB of SNR. Figure

4-13 shows the output spectrum of our modulator with a full scale 20kHz sinusoidal input. And Figure 4-14 shows the quantization noise shaping characteristic of our modulator using zero input voltage.

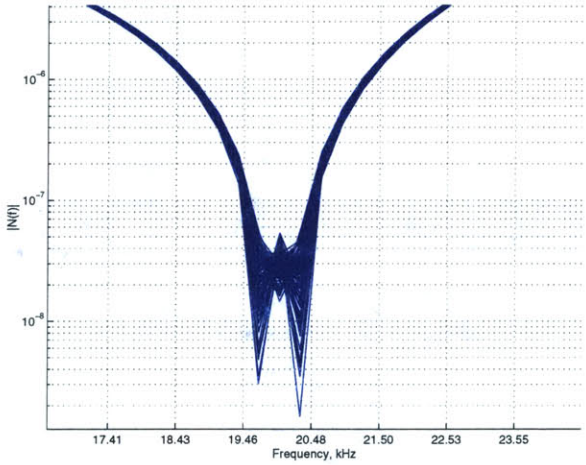

Figure 4-11: Noise Transfer Function Frequency Response showing Effects of Capacitor Mismatch

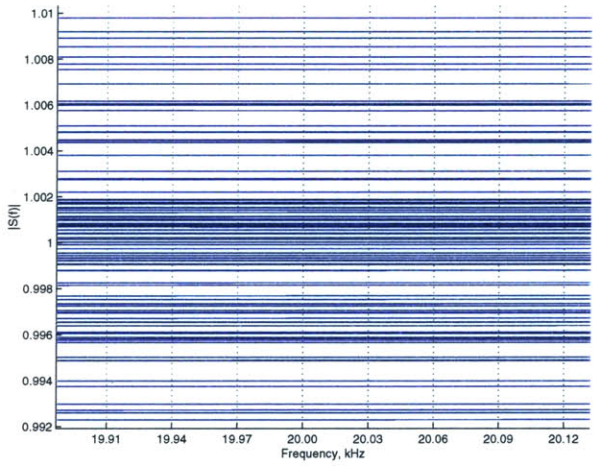

Figure 4-12: Signal Transfer Function Frequency Response showing Effects of Capacitor Mismatch

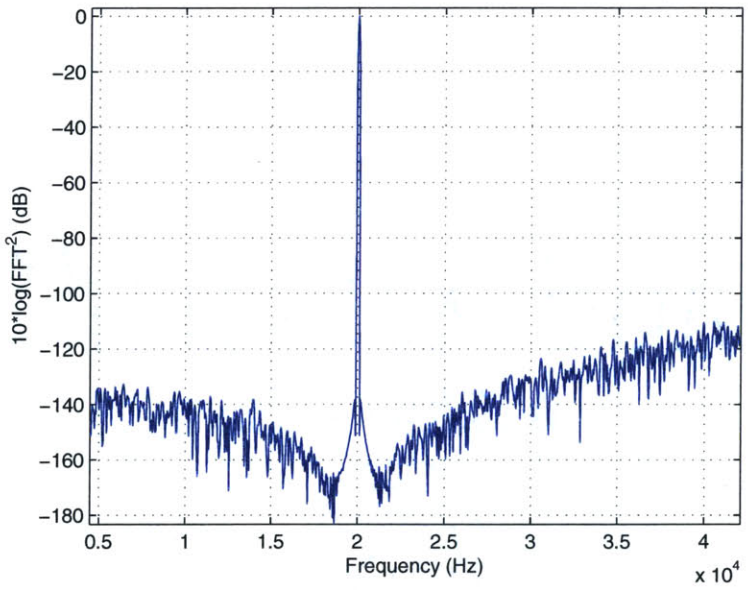

Figure 4-13: Output Frequency Spectrum for 20kHz Full-Scale Sinusoidal Input

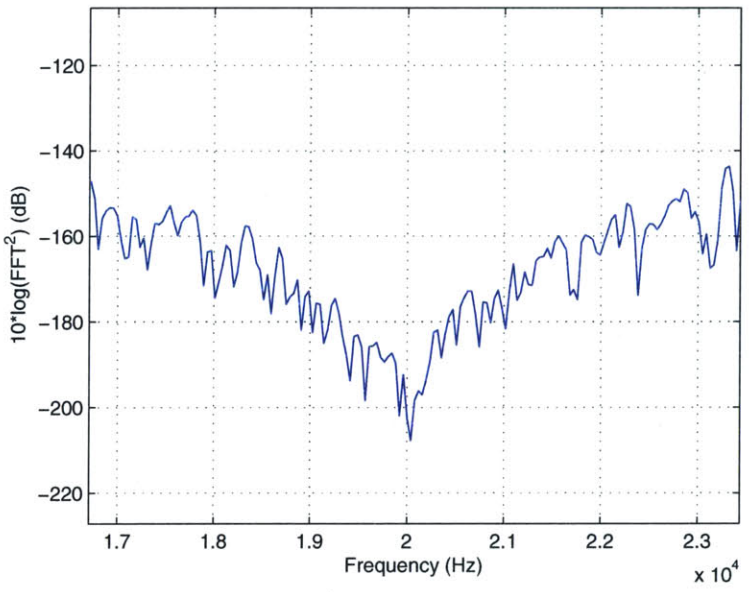

Figure 4-14: Output Frequency Spectrum for Zero Input

Chapter 5

$\Sigma\Delta$ Integrator Enhancement

The performance of the input integrator in a $\Sigma\Delta$ modulator is one of the most critical factors in determining the overall converter performance. The reason for this importance is that since the integrating opamp is designed to have a considerable amount of gain (usually $>$ 60dB), the baseband noise contribution of the succeeding integrators will be highly attenuated when referred back to the modulator's input [8]. Hence careful design of the first-stage integrator is crucial because its associated errors show up directly at the input to our modulator.

In Chapter 3, we saw how the flicker noise in the first integrator was the limiting factor in the converter's noise performance. Additionally, the graduate thesis work of Keith Santarelli illustrated how voltage offset between the two opamp input terminals can result in a gain error in the integrator's transfer function [3]. Both of these errors result from imperfections in the IC fabrication process. The former stems from traps present in the MOS transistors' gate oxide that impact carrier transit in the devices conducting channel. The latter error primarily comes about from mismatch in the dimensions of the input transistors.

In this chapter, we discuss and quantify the beforementioned errors in the previous modulator's first stage integrator with respect to the overall modulator peformance. Furthermore, we propose a new integrator structure that is capable of greatly reducing the impact of these error sources. This new integrator structure is implemented and simulated in HSPICE. Finally, the results of these simulations are presented in

comparison to the previous modulator's first stage integrator in order to assess the benefits that accompany this change in structure.

5.1 Input Voltage Offset and Flicker Noise in a Switched-Capacitor Integrator

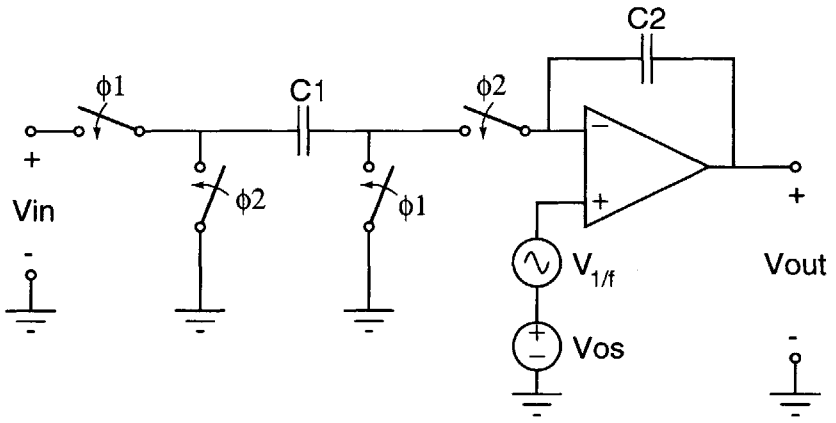

Figure 5-1: A Single-Ended Version of the Previous Modulator's Integrator Structure

The structure of the previous modulator's first stage integrator is shown in Figure 5-1. When the opamp that comprises this integrator is ideal, the voltage sources that we place on its noninverting terminal can be set equal to zero. The operation of this switched capacitor circuit is as follows. During ϕ_1, capacitor C_1 is charged to V_{in} and the output voltage is sampled by the second stage integrator (Not Shown). On the next phase, $\phi 2$, C_1 is connected in an inverting configuration with the integrating capacitor, C_2. With the terminal of C_1 that was connected to the input signal now connected to ground, we see a charge dump from C_1 onto C_2 that results in a rising V_{out} for a positive sampled input voltage. The transfer function of this integrator is given by:

$$V_{out}(z) = \frac{C_1}{C_2} \frac{z^{-1}}{1 - z^{-1}} V_{in}(z) \tag{5.1}$$

One of the key assumptions that we made in obtaining the above transfer function was that the opamp was ideal. That is $v_+ = v_-$, which equals zero in the above

circuit. Infinite opamp gain and negative feedback ensures this is the case in an ideal integrator. However, in practice, the gain of the opamp is finite and a small difference in the voltage across the opamp's input terminals is necessary to obtain a given output voltage. This voltage is one contributor to the *offset voltage* and it is modeled as a DC voltage source of value V_{out}/A, where A is the gain of the amplifier, in series with either of the opamp terminals as shown in Figure 5-1.

Finite opamp gain is not the only factor in determining the magnitude of this offset voltage. The degree to which the two halves of the circuit (i.e. v_+ to output and v_- to output) are matched affects the offset voltage as well. In simulation, it is possible to match both of these halves perfectly and the offset voltage would be solely due to finite opamp gain. In reality, this will certainly never be the case. In a fabricated differential circuit, the dimensions of the transistors in each differential half circuit are subject to process errors and therefore will not be perfectly matched. Again, the effects of these differences can be modeled as a voltage source in series with either of the opamp terminals. That is we can add it to the offset voltage due to finite opamp gain.

We can obtain values for the input offset voltage due to finite opamp gain and transistor mismatch via simulation in HSPICE. Connecting an opamp with matched positive and negative half circuits in a unity-gain configuration, allows us to obtain the magnitude of the offset voltage which is due to finite opamp gain. This value is found to be 100μV. Since the input differential pair of a well-designed opamp provides a large amount of gain, the errors due to transistor mismatch in stages following the first will result in negligible offset voltage compared to that which originates from the input pair. Thus we can vary the lengths and widths of the opamp's input differential pair according to the specified process tolerances to get an estimated value for the expected offset voltage due to transistor mismatch. Monte carlo simulation option in HSPICE allows us to vary a given paramenter (i.e. voltage, resistance, transistor width, etc) randomly given some statistiscal properties (probability density function, mean, and variance) for the certain element. After performing the simulations that we just described, we find that the offset voltage due to transistor mismatch can be

be on the order of 5mV.

We now consider the effect of the opamp's offset voltage on the transfer function of the integrator in Figure 5-1. With the errors due to finite opamp gain and mismatch modeled as a DC voltage source V_{os} in series with the noninverting opamp terminal of value $V_{out}/A + V_{mismatch}$, we can again make the assumption that $v_+ = v_-$. Therefore the inverting terminal of of the opamp is at V_{os} and the charge transfer from C_1 to C_2 is proportional to $V_{in} - V_{os}$. We now derive the transfer function of the integrator. At the end of ϕ_1 at time nT-T, the charge on C_1 is equal to $C_1 V_{in}(nT - T)$ and the charge on C_2 is:

$$Q_{C2}(nT - T) = C_2(V_{out}(nT - T) - \frac{V_{out}(nT - T)}{A}) - V_{mismatch} \tag{5.2}$$

During the following integration phase, ϕ_2, the charge change on C_1 results in an increase in charge on C_2 which is equal to:

$$\Delta Q_{C2}(nT - T/2) = C_1(V_{in}(nT - T) - \frac{V_{out}(nT - T)}{A} - V_{mismatch}) \tag{5.3}$$

At the end of the next phase, ϕ_1, the output voltage is given by:

$$V_{out}(nT) = \frac{V_{out}(nT)}{A} + V_{mismatch} + V_{C2} \tag{5.4}$$

where $V_{C2} = \frac{Q_{C2}(nT-T)+\Delta Q_{C2}(nT-T/2)}{C_2}$. Changing the variables to discrete-time by setting n=nT and taking the z-transform yields the following transfer function:

$$V_{out}(z) = \frac{\frac{C_1}{C_2}(V_{in}z^{-1} - V_{mismatch})}{(1 - \frac{1}{A}) - (1 - \frac{1}{A}(1 + \frac{C_1}{C_2}))z^{-1}} \tag{5.5}$$

For the case of $A >> 1$ and $V_{mismatch} = 0V$, we see that the above equation reduces to Equation 5.1, which is the transfer function of our integrator structure with an ideal integrator. Otherwise, we see that the DC gain (i.e. $|V_{out}(z = 1)|$) of our integrator is no longer infinity and that the offset voltage due to transistor mismatch is integrated along with the input voltage. This last point means that the error due to transistor

mismatch shows up directly at the integrator's input without being attenuated. Since the gain of the opamp that we employ in our integrating structure is on the order of 80dB, in our analysis we neglect the finite op-amp gain error and focus on the error due to transistor mismatch. We now look to simulation to give us insight as to how transistor mismatch alters the performance of our integrator.

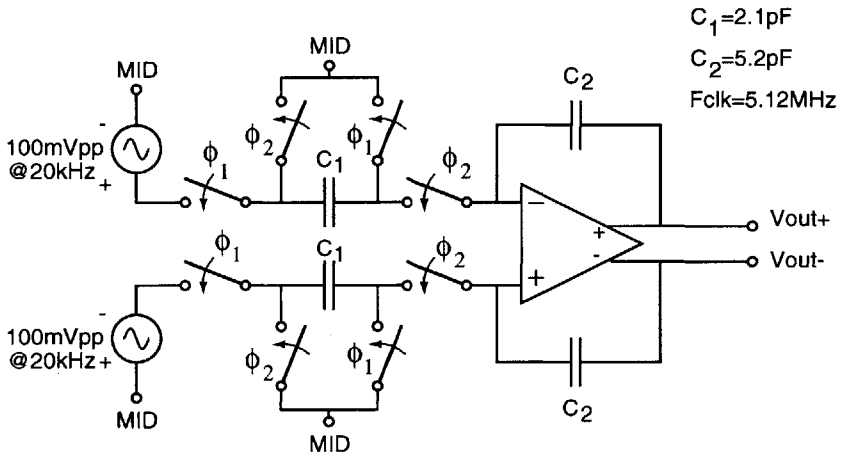

Figure 5-2: Fully-Differential Integrator used for Offset Voltage and 1/f Noise Simulations

Figure 5-2 shows the fully-differential, switched-capacitor integrator that we employ to observe the effects of the opamp's input offset voltage on the peak-to-peak amplitude of the output voltage.[1] We employ ideal switches so that we can isolate the opamp errors. The circuit is run off of a 5V power supply and contains a virtual ground (MID=2.5V) about which the input and output signals are centered. When taken differentially, the two sinusoidal voltage sources form a 200mV_{pp} input to our integrator. These sources are not turned on until t=$10\mu s$. Hence for the first $10\mu s$ of simulation, the opamp's offset voltage is integrated.[2] This $10\mu s$ period simply lets us view the integration of the opamp's offset voltage and how it changes the output over time. At t=$10\mu s$, the input voltage sources are turned on and the simulation is until t=$50\mu s$. We display the output waveforms of this circuit for input offset voltages

[1]In simulation, we determined the offset voltage due to the finite gain error to be negligible compared to that seen when the transistor widths were varied in monte carlo simulation which is on the order of a few millivolts. This result makes sense as the gain of the opamp is so large ($\approx 80dB$).

[2]The DC voltage source which we place in series with the inverting opamp terminal is not shown in the circuit in Figure 5-2.

of 100μV, 500μV, 1mV, 5mV and 10mV in Figure 5-3. The ideal transfer function predicts a gain of 16.45 at 20kHz for the our circuit. This prediction would result in an output voltage $V_{out} = 3.29V_{pp}$. However, as shown in Table 5.1, the opamp's offset voltage can cause 20% deviations from the ideal peak-to-peak output value. This large gain error makes the utilization of the previous integrator structure unattractive as it requires us to account for these nonidealities in the noise-shaping loop, which makes the design of our modulator more complex. The gain error effectively reduces the gain of the integrator blocks and therefore increases the quantization noise power in the band of interest. Hence, we might need to consider redesigning our noise-shaping loop so that it is robust against these errors that stem from limitiations of the IC fabrication process which are difficult to model. In a moment, we will see how we can make our integrator structure more tolerant to these process errors, thus avoiding the need to reconsider the the design of our modulator's noise transfer function.

V_{os}	$V_{out,pp}$
100μV	3.29V
500μV	3.26V
1mV	3.22V
5mV	2.93V
10mV	2.57V

Table 5.1: Peak to Peak Output Voltage Measurements for Various Input Offset Voltages in the Circuit of Figure 5-2

In addition to modeling the finite gain and transistor mismatch of the previous integrator's structure with a voltage source in series with one of the opamp terminals, we can model the flicker (1/f) noise of the opamp as a time-varying voltage source at one of the opamp inputs as shown in Figure 5-1[3]. Chapter 3 showed us how this noise source is the dominant noise source in the previous modulator with an inband noise density of 145nV/$\sqrt{\text{Hz}}$. This is because the opamp's flicker noise is not attenuated when it is referred to the input; rather, it is integrated along with the input voltage as the following analysis shows.

[3]In our simulations, this noise source is modeled as a 20kHz sine wave in series with the non-inverting opamp input. Given just an HSPICE simulator, this technique to model the opamp's flicker noise was the only method possible.

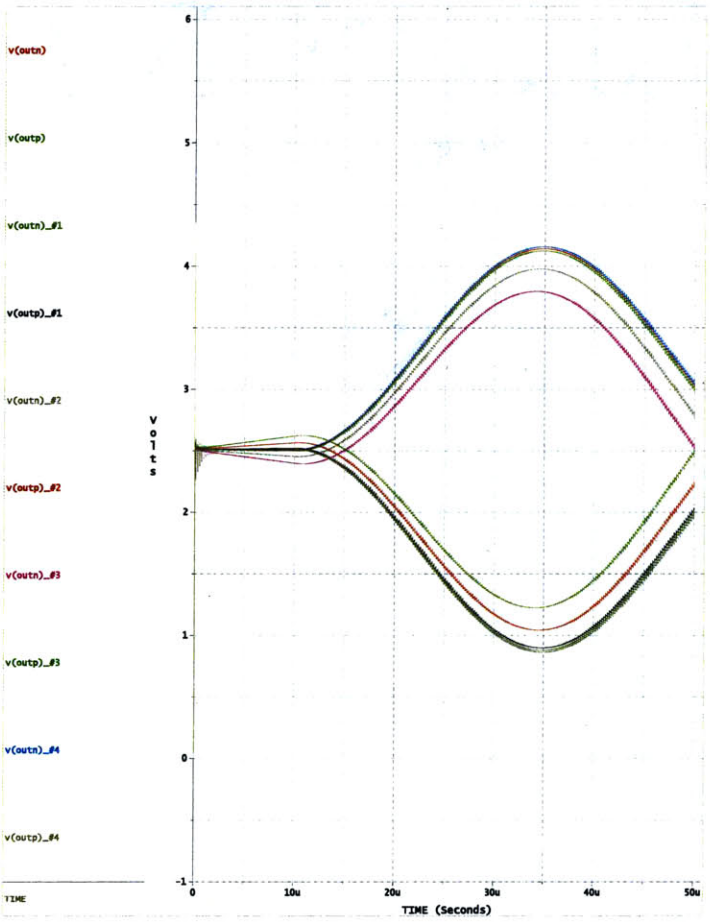

Figure 5-3: Impact of DC Offset Voltage on Previous Integrator Structure with a 200mV_{pp} Differential Sine Wave Input. Pairs of labels on the y-axis (i.e. v(outn) and v(outp) indicate the fully-differential outputs for a certain offset voltage simulation.

Let us see mathematically how the opamp's 1/f noise shows up at the output of the integrator with reference to the structure in Figure 5-1. We are interested in finding the output voltage at some time nT (i.e. $V_{out}(nT)$) due to the time varying voltage $V_{1/f}(nT)$ in series with the opamp's noninverting input (i.e. The input voltage source is set to zero). At the end of the previous clock cycle's ϕ_1, time nT-T, the charge on capacitor C_2 is given by:

$$Q_2(nT-T) = C_2(V_{out}(nT-T) - V_{1/f}(nT-T)) \tag{5.6}$$

With the input set equal to zero, at the end of ϕ_2 (time nT-T/2), the change of the charge on C_1 can be expressed as

$$\Delta Q_1 = C_1 V_{1/f}(nT-T/2) \tag{5.7}$$

Since the charge at any node is conserved and the opamp has infinite input impedance, $\Delta Q_1 = \Delta Q_2$. Therefore the total charge on C_2 at the end of ϕ_2 is:

$$Q_2 = C_2(V_{out}(nT-T) - V_{os}(nT-T)) + C_1 V_{os}(nT-T/2) \tag{5.8}$$

The output of our circuit is valid at the end of ϕ_1 (time nT) where we have the relation:

$$V_{out}(nT) = V_{1/f}(nT) + V_{C2}(nT) \tag{5.9}$$

where $V_{C2}(nT) = \frac{Q_{nT}}{C_2}$ and we get the following expression:

$$V_{out}(nT) - V_{out}(nT-T) = V_{1/f}(nT) - V_{1/f}(nT-T)) + \frac{C_1}{C_2} V_{1/f}(nT-T/2) \tag{5.10}$$

Substituting the discrete-time variables $V_{out}(n)$ and $V_{1/f}(n)$ in for $V_{out}(nT)$ and $V_{1/f}(nT)$ and taking the z-transform yields the following transfer function:

$$\frac{V_{out}}{V_{1/f}}(z) = \frac{1 - z^{-1} + \frac{C_1}{C_2} z^{-\frac{1}{2}}}{1 - z^{-1}} \tag{5.11}$$

From the equation above, we can see that the $z^{-\frac{1}{2}}$ term will dominate the numerator if the sampling rate is much higher than the bandwidth of $V_{1/f}$ (i.e. $V_{1/f}(nT) \approx V_{1/f}(nT - T)$ in Equation 5.10). Thus we see that the low frequency (1/f) noise of our opamp will be integrated along with the input voltage. The magnitude of Equation 5.11 verses frequency is shown in Figure 5-4.

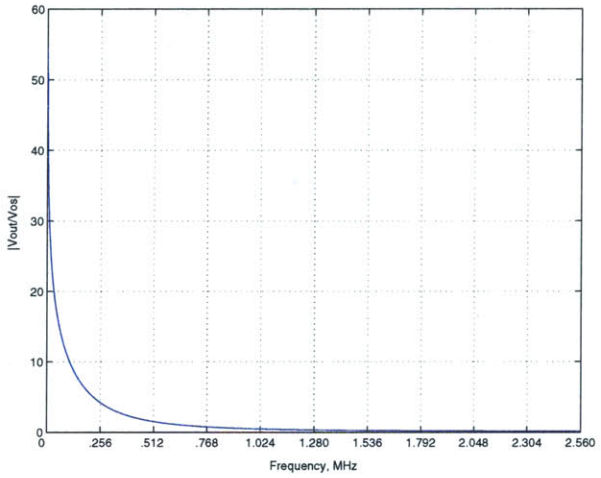

Figure 5-4: Magnitude of V_{out}/V_{os} as a Function of Frequency

Figure 5-5 illustrates this point in simulation. To obtain these output waveforms, we set the input sources to zero and connect a 20kHz sinusoidal source in series with the inverting terminal of the opamp in the circuit of Figure 5-2. In Figure 5-5 and Table 5.2 we can see how this time-varying offset voltage is gained up by the same factor of 16.45 that the input experienced in the case of an ideal integrator.

$V_{os,pp}$	$V_{out,pp}$
10mV	167.8mV
20mV	335.2mV
50mV	837.2mV
100mV	1.67V
200mV	3.33V

Table 5.2: Peak to Peak Output Voltage Measurements for 20KHz Sinusoidal Input Offset Voltages in the Circuit of Figure 5-2

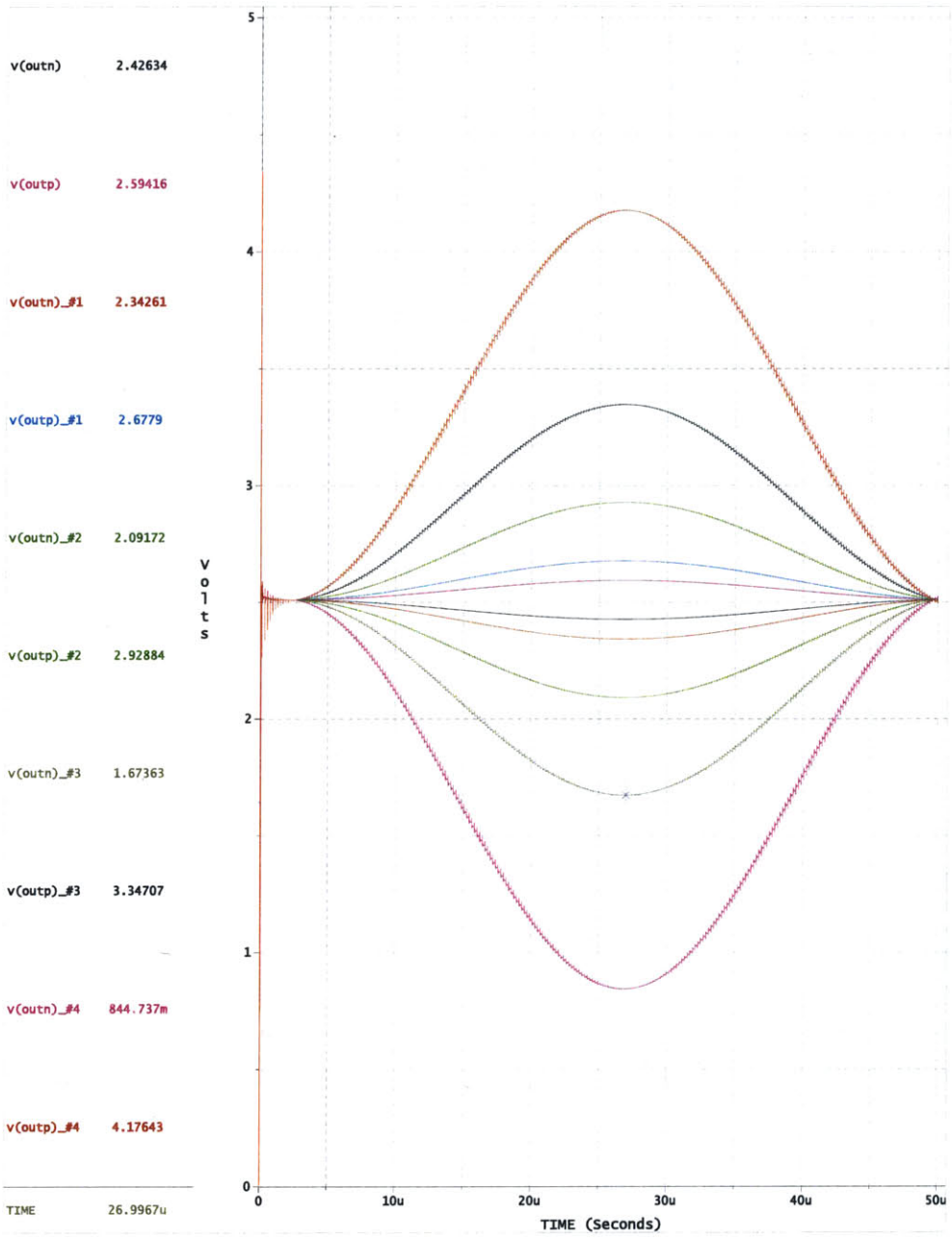

Figure 5-5: Impact of Time-Varying Offset Voltage on Previous Integrator Structure

5.2 Correlated Double Sampling

Given the known SNR performance impact of the opamp's flicker noise on the previous modulator and the integrator's susceptibility to gain errors due to random process mismatch, we propose a new integrator for use in our improved modulator. The structure of this new integrator is shown below in Figure 5-6.

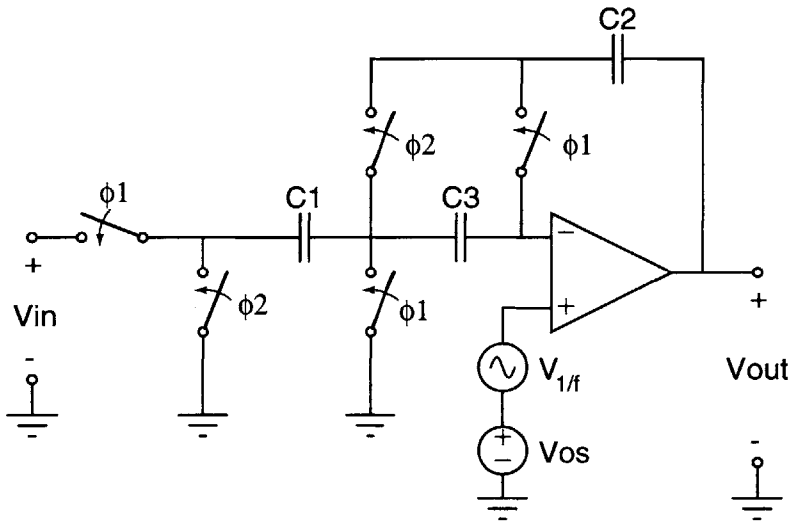

Figure 5-6: Single-Ended Integrator with Correlated Double Sampling for Improved Modulator

With the addition of one switch and one capacitor, we will find that we can drastically decrease our integrator's vulnerability to the error sources described in the previous section. The operation of the above circuit is as follows. During ϕ_1, capacitor C_1 samples the input voltage and the capacitor C_3 samples the opamp's offset voltage V_{os}. During ϕ_2, the integration is performed as the charge on C_1 is transferred to the integrating capacitor C_2, while the DC offset and the low frequency 1/f noise of the amplifer are cancelled by the voltage stored on C_3. This cancellation during the integration phase results from C_3 being placed in series with the opamp's inverting terminal, thereby making the charge transfer nearly independent of the opamp's inverting terminal voltage. This technique for compensating for the finite offset voltage of the integrating opamp is termed correlated double sampling and is routinely employed in high-precision $\Sigma\Delta$ modulators [6], [14], [18].

In order to quantify the benefits that the integrator structure in Figure 5-6 gives us, we find the transfer function from the time-varying offset voltage to the output voltage. We begin by finding the charge on each capacitor at the end of ϕ_1 at time nT-T:

$$Q_C(nT-T) = \begin{cases} C_1 V_{in}(nT-T) & \text{for } C_1 \\ C_2(V_{out}(nT-T) - V_{os}(nT-T)) & \text{for } C_2 \\ C_3 V_{os}(nT-T) & \text{for } C_3 \end{cases}$$

During ϕ_2, the offset storage capacitor C_3 acts like a battery with voltage $V_{os}(nT-T)$. C_3 does not dump any charge in this phase because it is connected in series with the opamp's inverting terminal and thus no current can flow onto or off it. Also, due to the series connection of C_3 with the inverting opamp input, the charge dump onto the integrating capacitor C_2 due to C_1 is proportional to $V_{in}(nT-T) - V_{os}(nT-T/2) + V_{os}(nT-T)$. Hence, at the end of ϕ_2 which is time nT-T/2, the charge on each capacitor is given by:

$$Q_C(nT-T/2) = \begin{cases} C_1(V_{os}(nT-T) - V_{os}(nT-T/2)) & \text{for } C_1 \\ C_2(V_{out}(nT-T) - V_{os}(nT-T)) + C_1(V_{in}(nT-T) & \\ \quad -V_{os}(nT-T/2) + V_{os}(nT-T)) & \text{for } C_2 \\ C_3 V_{os}(nT-T) & \text{for } C_3 \end{cases}$$

During the following phase, ϕ_1, there is an additional charge dump from C_3 onto C_2 that is proportional to $V_{os}(nT) - V_{os}(nT-T)$. At the end of this phase the time is nT and we can express the output voltage as:

$$V_{out}(nT) = V_{os}(nT) + V_{C2}(nT) \tag{5.12}$$

which leads to the following difference equation:

$$\begin{aligned} V_{out}(nT) - V_{out}(nT-T) &= V_{os}(nT) - V_{os}(nT-T) - \frac{C_1}{C_2}\left(V_{os}(nT-T/2) - V_{os}(nT-T)\right) \\ &\quad - \frac{C_3}{C_2}\left(V_{os}(nT) - V_{os}(nT-T)\right) + \frac{C_1}{C_2}\left(V_{in}(nT-T)\right) \end{aligned} \tag{5.13}$$

Setting $V_{in} = 0$ for all time, substituting the discrete-time variables $V_{out}(n)$ and $V_{os}(n)$ in for $V_{out}(nT)$ and $V_{os}(nT)$ and taking the z-transform yields the following transfer function:

$$\frac{V_{out}}{V_{os}}(z) = \frac{1 - z^{-1} - \frac{C_1}{C_2}(z^{-\frac{1}{2}} - z^{-1}) + \frac{C_3}{C_2}(1 - z^{-1})}{1 - z^{-1}} \tag{5.14}$$

As seen in Figure 5-7, we have a high-pass response from the offset voltage source to the output. Recall from the previous section that the old integrator structure caused the offset voltage to be integrated! The plot in Figure 5-7 tells us that offset voltages with frequencies that are much lower than the sampling frequency will exhibit a gain of about 0.8 to the output.[4]

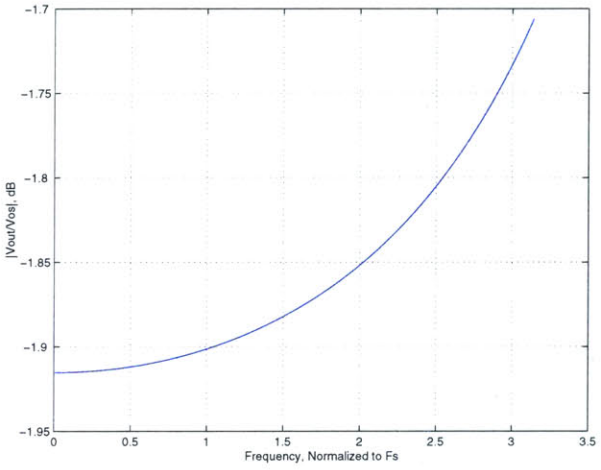

Figure 5-7: Magnitude of V_{out}/V_{os} as a Function of Frequency

So now we can quantify the impact of this new integrator structure on our modulator's inband noise level. At 20kHz, the flicker noise density for our opamp is $154\text{nV}/\sqrt{\text{Hz}}$. In the previous integrator structure, we saw how this noise is gained up by a factor of about 16 to the output, which is the same amount of gain that the input voltage experiences. Therefore, the opamp's flicker noise can be referred back to the input without any attenuation. In our new integrator structure, the low-frequency noise of the op-amp is experiences a gain of 0.8 to the output. Thus, when referred

[4]Plot created for $C_1 = C_2 = 2.1\text{pF}$ and $C_3 = 5.2\text{pF}$.

back to the input, the opamp's flicker noise is attenuated by a factor of 20 and this noise source has an inband noise density of $7.7\text{nV}/\sqrt{\text{Hz}}$.

Moreover, the gain error in the previous integrator structure due to finite opamp gain and transistor mismatch is eliminated. Looking at Equation 5.13, we see that since the offset voltage is DC, which is how we model these two nonidealities, then the output voltage is immune to these errors.

We use the circuit in Figure 5-8 to simulate the new integrator structure in HSPICE. As in the previous section we use ideal switches so that the opamp is the sole source of nonidealities in our circuit. The simulations are also run as we described in the previous section for the case of a pure DC offset and then the case of a time-varying offset. The results of these tests are depicted in the following figures.

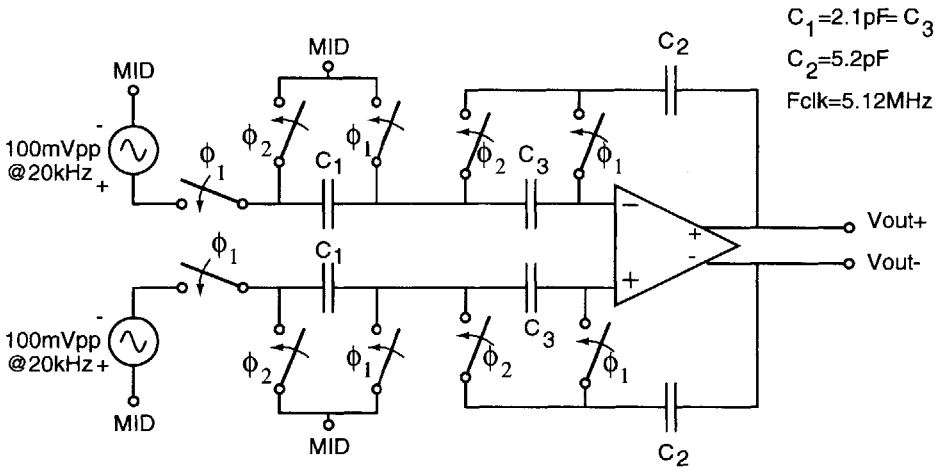

Figure 5-8: Improved Fully-Differential Integrator used for Offset Voltage and 1/f Noise Simulations

V_{os}	$V_{out,pp}$
100μV	3.32V
500μV	3.32V
1mV	3.32V
5mV	3.32V
10mV	3.32V

Table 5.3: Peak to Peak Output Voltage Measurements for Various Input Offset Voltages in the Circuit of Figure 5-8

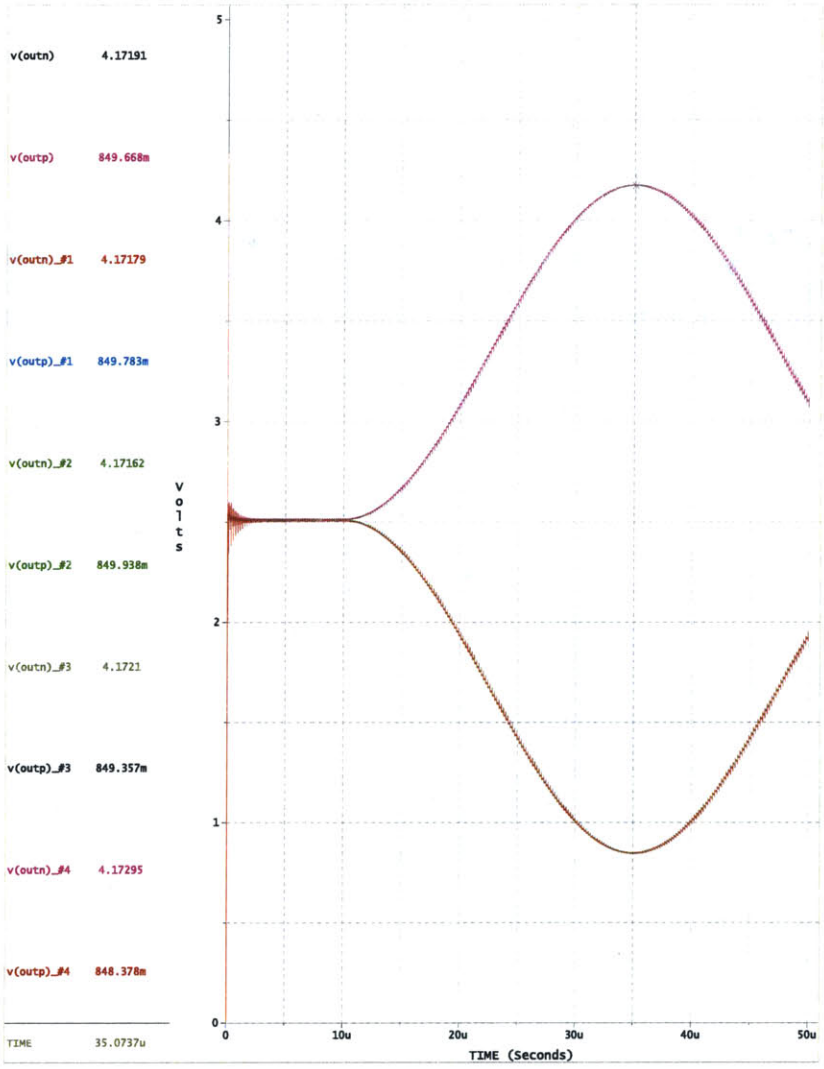

Figure 5-9: Impact of Offset Voltage on Improved Integrator Structure

$V_{os,pp}$	$V_{out,pp}$
10mV	8.34mV
200mV	17.11mV
50mV	38.54mV
100mV	67.18mV
200mV	130.66mV

Table 5.4: Peak to Peak Output Voltage Measurements for 20kHz Sinusoidal Input Offset Voltages in the Circuit of Figure 5-8

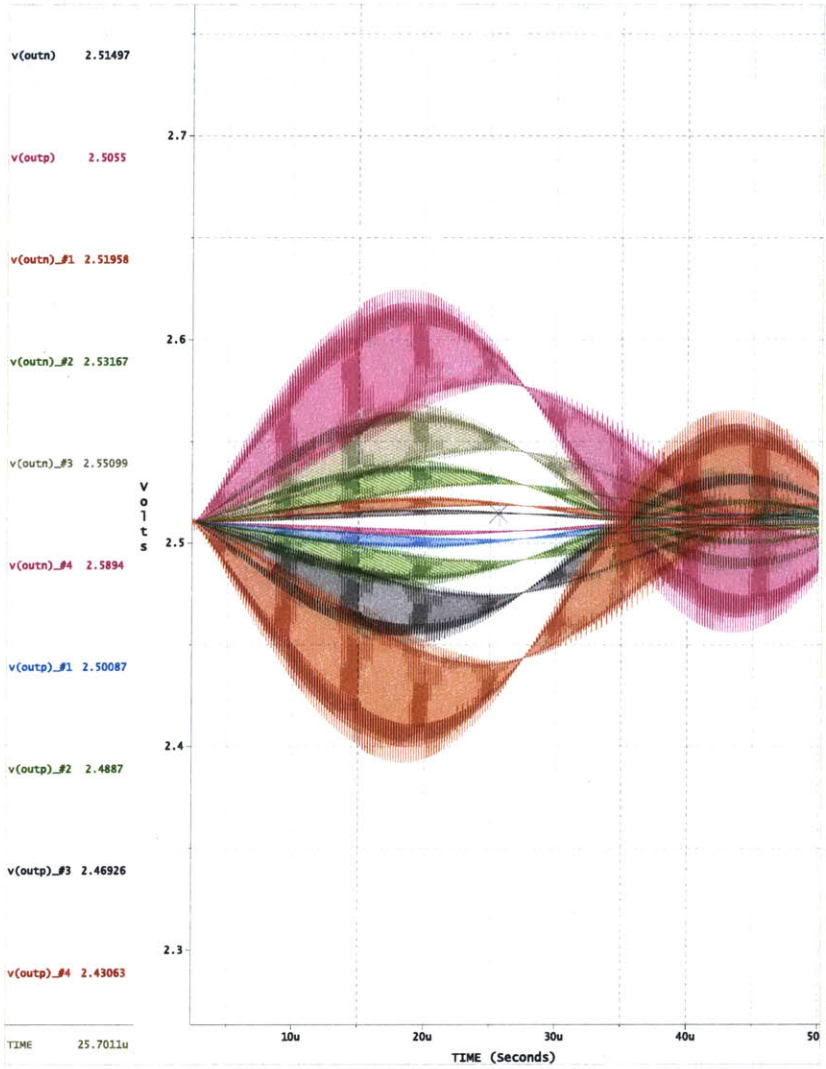

Figure 5-10: Impact of Time-Varying Offset Voltage on Improved Integrator Structure

5.3 Proposed Integrator Implementation Issues

When it comes time to implement our correlated double sampling scheme using real switches, we find that switch nonidealities greatly impact the integrators performance. This impact manifests itself mainly in terms of an offset error. This error stems from the fact that our switches have some finite "on" resistance which results in incomplete charge transfers during each phase. Because of these incomplete charge transfers our integrator structure can never fully compensate for the offset voltage. While the curves in Figure 5-11 appear not to be affected by the offset voltage, Table 5.5 reveals that this is not the case. For a 10mV DC offset, our output signal's amplitude is in error by 1%. This is still a major improvement over the 20% error for this same offset voltage in the previous integrator structure. And with this error on the order of 1%, we are not forced to go back and remodel the integrator blocks in Figure 4-8. Turning to the case when the offset voltage is time-varying to simulate the opamp's flicker noise, we see in Figure 5-12 that the DC offset voltage due to the incomplete charge transfer causes our outputs' DC level to shift 500mV over $50\mu s$. However, if we look at the figure closely, we observe that the peak-to-peak amplitude of the individual waveforms is attenuated by roughly this same 0.8 factor that we saw previously. This means that when we refer the opamp's flicker noise to our modulator input, it will still be highly attenuated.

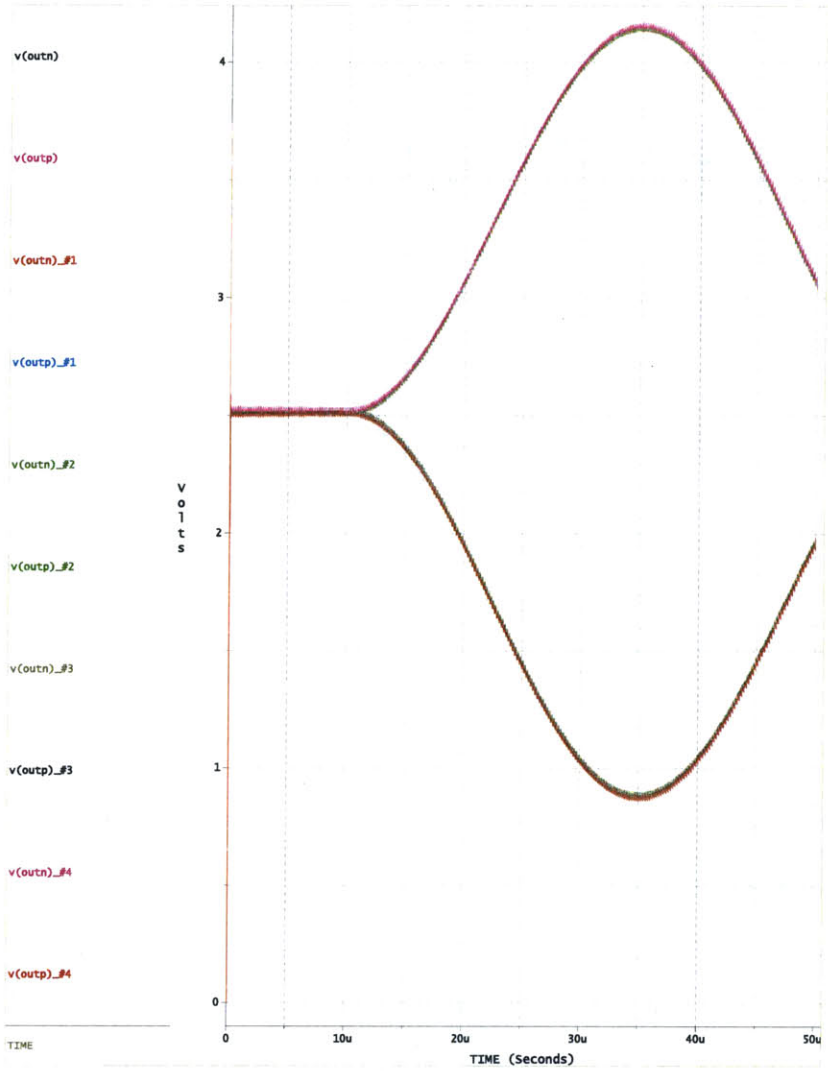

Figure 5-11: Impact of Offset Voltage on Improved Integrator Structure with Nonideal Switches

V_{os}	$V_{out,pp}$
100μV	3.254V
500μV	3.255V
1mV	3.257
5mV	3.270V
10mV	3.287V

Table 5.5: Peak to Peak Output Voltage Measurements for Various Input Offset Voltages in the Circuit of Figure 5-8 with Nonideal Switches

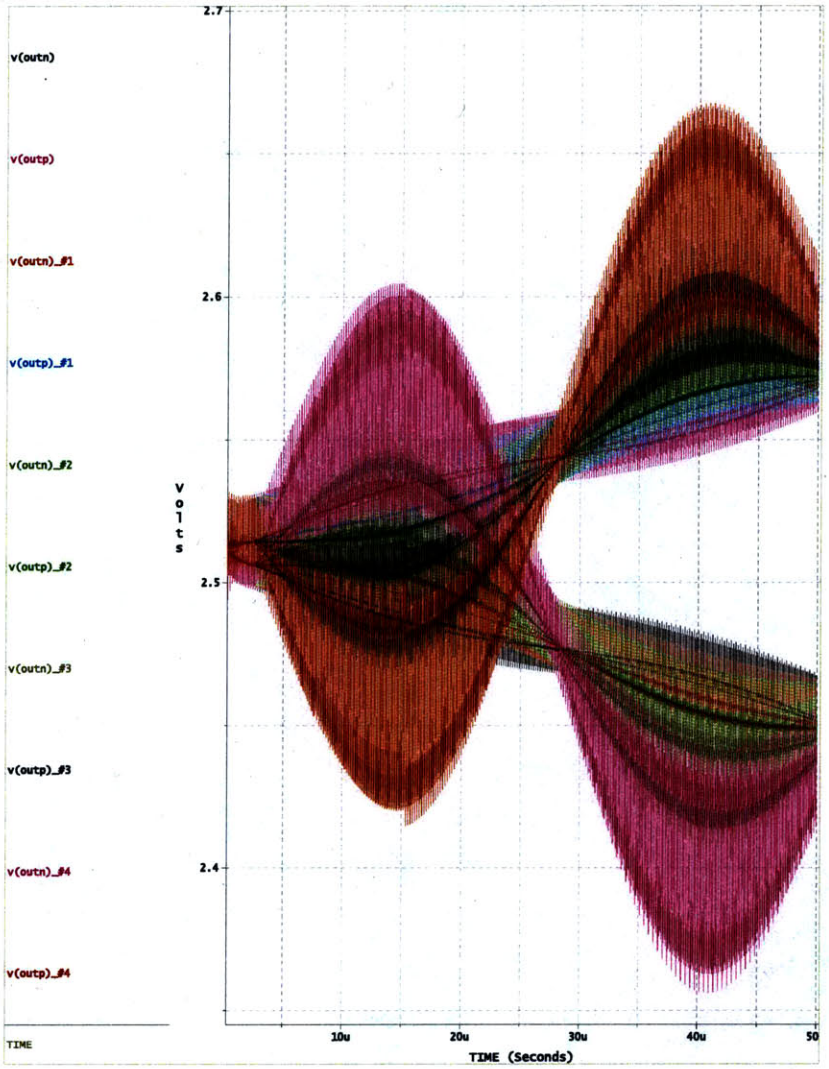

Figure 5-12: Impact of Time-Varying Offset Voltage on Improved Integrator Structure with Nonideal Switches

$V_{os,pp}$	$V_{out,pp}$
10mV	-
200mV	-
50mV	-
100mV	62.92mV
200mV	160.08mV

Table 5.6: Peak to Peak Output Voltage Measurements for 20kHz Sinusoidal Input Offset Voltages in the Circuit of Figure 5-8 with Nonideal Switches

Chapter 6

Conclusion and Recomendations for Future Work

In this document, we submitted a plan to increase the signal to noise ratio of a third-order, discrete-time $\Sigma\Delta$ modulator. Because this previous modulator achieves acceptable levels of performance in current applications at Draper Laboratory, we decided to use it as a starting point for our improved modulator. In Chapter 3, our analysis of the previous modulator found that the opamp's flicker noise is the dominant inband noise source. Moreover, by setting the kT/C noise ($40\text{nV}/\sqrt{\text{Hz}}$) to be our modulator's noise floor, we created a need to further attenuate the inband quantization noise in addition to reducing the amount of flicker noise that gets input-referred. Chapter 4 walked us through the design methodology of the fourth-order, bandpass modulator transfer function that we employ to attain this reduction in quantization noise from $41\text{nV}/\sqrt{\text{Hz}}$ to $0.4\text{nV}/\sqrt{\text{Hz}}$. And Chapter 5 presents a front-end integrator structure that serves to attenuate the amount of input-referred flicker noise from the integrator's operational amplifier. Matlab analysis and HSPICE simulation showed this new integrator structure reduces the inband flicker noise by a factor of 20 down to approximately $7\text{nV}/\sqrt{\text{Hz}}$. With no change in the sampling and opamp thermal noise densities ($40\text{nV}/\sqrt{\text{Hz}}$ and $53\text{nV}/\sqrt{\text{Hz}}$, respectively), our modulator's inband

noise density is given by:

$$V_{n,rms} = \sqrt{(40 \times 10^{-9})^2 + (53 \times 10^{-9})^2 + (0.4 \times 10^{-9})^2 + (7 \times 10^{-9})^2} \quad (6.1)$$

$$= 66.7nV/\sqrt{\text{Hz}} \quad (6.2)$$

where all the quantities in 6.1 are in $\text{V}/\sqrt{\text{Hz}}$. Thus we have met our application's noise specification of $80\text{nV}\sqrt{\text{Hz}}$. However, we notice that our circuit's noise floor is not set by kT/C noise as the aliased opamp thermal noise is at $53\text{nV}/\sqrt{\text{Hz}}$. With the opamp's flicker noise no longer a major concern because we employ correlated double sampling, future modulator work should investigate the utilization of n-channel devices in the opamp's input differential pair to decrease the opamp's thermal noise density. This change would increase the transconductance of each transistor in the differential pair and each devices thermal noise current will experience increased attenuation when referred to the input as a voltage.

Future work should also consist of examining whether some of the feedforward paths in our modulator structure of Figure 4-8 could be eliminated. These paths create zeros in the signal transfer function in order to make its gain flat (approximately unity) over the band of interest to the converter's overall accuracy. However, it might be possible to remove some of these zeros and compenensate for any gain changes over this band of interest in the digital realm. This shift in signal processing would reduce the size and complexity of the analog modulator.

Lastly, since we were restricted to only performing transient simulations in HSPICE due to the sampled nature of our system, we had to use hand calculations to predict the overall noise performance of the improved modulator. Thus, it is imperative that future modulator efforts employ tools that more accurately predict the performance impact of the various modulator noise sources. Spectre would allow us to simulate noise in switched-capacitor circuits which are the building blocks of our modulator. And with its ability to capture the exact behavior of a set of nonlinear difference equations, Simulink is also a powerful tool for modeling our system as we depicted in Chapter 4. In the future, we could construct a more comprehensive behavioral model

of our system that incorporates modulator nonidealities such as kT/C noise, opamp saturation voltages and opamp noise in the Simulink environment to obtain better performance estimates.

Bibliography

[1] M. W. Hauser, "Principles of Oversampling A/D Conversion," *J. Audio Eng. Soc.*, vol. 39, pp. 3-26, January/February 1991.

[2] P. W. Juang, "A Continuous Time Sigma-Delta Modulator for Digitizing Carrier Band Measurements," M.Eng. Thesis, Massachusetts Institute of Technology, Cambridge, MA, 2001.

[3] K. R. Santarelli, "A Low Power Digitizer for Precision Carrier Band Measurements," M.Eng. Thesis, Massachusetts Institute of Technology, Cambridge, MA, 2000.

[4] A. V. Oppenheim and A. S. Willsky with S. H. Nawab, *Signals & Systems*, 2nd ed., Upper Saddle River, New Jersey: Prentice Hall, 1997.

[5] D. A. Johns and K. W. Martin, *Analog Integrated Circuit Design.* New York: John Wiley & Sons, 1997.

[6] S. Rabii and B. Wooley, *The Design of Low-Voltage, Low-Power Sigma-Delta Modulators.* Boston: Kluwer Academic Publishers, 1999.

[7] A. B. Grebene, *Bipolar and MOS Analog Integrated Circuit Design.* Hoboken, New Jersey: John Wiley & Sons, 2003.

[8] S.R. Norsworthy, R. Schreier and G. C. Temes, *Delta-Sigma Data Converters: Theory, Design, and Simulation.* New York: IEEE Press, 1997.

[9] K. Lundberg, *BECOMING ONE WITH THE TRANSISTOR for Solid State Circuits*, Unpublished, 2003.

[10] R. Schreier, *The Delta-Sigma Toolbox Version 6.0*, http://www.mathworks.com/matlabcentral/fileexchange, 2003.

[11] E. Hildebrant (private communication), 2005.

[12] H. Lee (6.775 Lecture Notes), 2004.

[13] R. Schreier, "An Empirical Study of High-Order Single-Bit Delta-Sigma Modulators," *IEEE Trans. Circuits Syst.*, vol. 40, pp. 461-464, August 1993.

[14] L. A. Williams and B. A. Wooley, "A Third-Order Sigma-Delta Modulator with Extended Dynamic Range," *IEEE Journal Solid-State Circuits*, vol. 29, pp. 193-202, March 1994.

[15] K. Chao, S. Nadeem, W. Lee, and C. Sodini, "A higher order topology for interpolative modulators for oversampling A/D converters," *IEEE Trans. Circuits Syst.*, vol. 37, pp. 309-319, March 1990.

[16] K. Nagaraj, J. Vlach, T. Viswanathan and K. Singhal, "Switched-capacitor integrator with reduced sensitivity to amplifier gain," *Electronic Letters*, vol. 22, pp. 1103-1105, October 1986.

[17] I. Fujimori, K. Koyama, D. Trager, F. Tam and L. Longo, "A 5-V Single-Chip Delta-Sigma Audio A/D Converter with 111dB Dynamic Range," *IEEE Journal Solid-State Circuits*, vol. 32, pp. 329-335, March 1997.

[18] R. Naiknaware and T. Fiez, "142dB $\Delta\Sigma$ ADC with a 100nV LSB in a 3V CMOS Process," *IEEE 2000 Custom Integrated Circuits Conference*, pp. 5-8, 2000.

[19] K. Leung, E. Swanson and S. Zhu, "A 5V, 118dB $\Delta\Sigma$ Analog-to-Digital Converter for Wideband Digital Audio," *International Symposium on Solid-State Circuits Digest of Technical*, pp. 218-219, February 1997.

[20] D. Kasha, W. Lee and A. Thomsen, "A 16-mW, 120-dB Linear Switched-Capacitor Delta-Sigma Modulator with Dynamic Biasing," *IEEE Journal Solid-State Circuits*, vol. 34, pp. 921-926, July 1999.

[21] CS5394 117dB, 48kHz, Audio A/D Converter Datasheet, Cirrus Logic, Austin, Texas, May 1998.

[22] S. Brigati et al, "Modeling Sigma-Delta Modulator Non-Idealities in Simulink," *Proceedings of IEEE International Symposium on Circuits and Systems*, pp. 384-387, 1999.